3.5.1.

The Institution has several collaborations/linkages for Faculty exchange, Student exchange, Internship, Field trip, On-the- job training, research etc during the year

2021-2022

internships

PARVATHAREDDY BABUL REDDY
VISVODAYA INSTITUTE OF TECHNOLOGY & SCIENCE
(AUTONOMOUS)
KAVALI – 524201, S.P.S.R Nellore Dist., A.P. India. Ph: 08626-243930

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

1.3.4 Details of students undertaking field work/ internships

AY:-2021-22

Programme Name	Programme Code	List of students undertaking field projects / internships /student projects	Link to the relevant document
B.TECH EEE	02	KANUMA REDDY MONIKA	
B.TECH EEE	02	B.MADHAN	
B.TECH EEE	02	P.DHANESH	
B.TECH EEE	02	K.NITHISH KUMAR REDDY	
B.TECH EEE	02	A.VIJAY SAI KUMAR	
B.TECH EEE	02	A.VENU	
B.TECH EEE	02	SK.SANDHANI	
B.TECH EEE	02	SK.SULTHAN BHASHA	
B.TECH EEE	02	SK.JAKEE SHARIF	
B.TECH EEE	02	M.PRASAD REDDY	
B.TECH EEE	02	D.ABHINAYA	
B.TECH EEE	02	G.SREEJA	
B.TECH EEE	02	K.SANGEETHA	
B.TECH EEE	02	CH.NANI	
B.TECH EEE	02	SK.SHAMEER	
B.TECH EEE	02	D.V.RAMACHANDRAIAH	
B.TECH EEE	02	R.VENKATA MANU	
B.TECH EEE	02	K.VIJAYA SAI	
B.TECH EEE	02	V.LAKSHMI NARAYANA	
B.TECH EEE	02	S.VAMSI KRISHNA	
B.TECH EEE	02	K.VENKATESH	
B.TECH EEE	02	V.PAVAN KUMAR	
B.TECH EEE	02	K.VISHNU VARDHAN	
B.TECH EEE	02	S.TARUN	
B.TECH EEE	02	G.JASHUVA	
B.TECH EEE	02	J.KEERTHI	
B.TECH EEE	02	CH.SUNEEL	
B.TECH EEE	02	A.NAGENDRA REDDY	
B.TECH EEE	02	K.LIKITHA MADHAVI	
B.TECH EEE	02	Y.PRAVALLIKA	
B.TECH EEE	02	D.GANGADHAR	
B.TECH EEE	02	M.RAVI TEJA	
B.TECH EEE	02	R.MEGHANA	
B.TECH EEE	02	D.MAHITH	
B.TECH EEE	02	B.SARITHA	
B.TECH EEE	02	A.SUJITHA	
B.TECH EEE	02	B.PRAVENN KUMAR	
B.TECH EEE	02	S.RENUKA	
B.TECH EEE	02	K.AMULYA	
B.TECH EEE	02	P.UMESH CHAND	
B.TECH EEE	02	E.RAJU	
B.TECH EEE	02	D.VISHITHA	
B.TECH EEE	02	V.PRAVALLIKA	
B.TECH EEE	02	V.SANDEEP	
B.TECH EEE	02	T.PRAVEEN	
B.TECH EEE	02	SK.YASIN	
B.TECH EEE	02	R.YASWANTH	
B.TECH EEE	02	R.MAHENDRA SIMHA	
B.TECH EEE	02	T.RAMAKRISHNA	

Programme Name	Programme Code	List of students undertaking field projects / internships /student projects	Link to the relevant document
B.TECH EEE	02	A.VENKATESH	
B.TECH EEE	02	E.SRINADH	
B.TECH EEE	02	P.VENKATESWARLU	
B.TECH EEE	02	S.V.SATWIKA	
B.TECH EEE	02	M.IMMANUEL	
B.TECH EEE	02	N.SIVA KAVITHA	
B.TECH EEE	02	D.SARANYA	
B.TECH EEE	02	K.ANUSHA	
B.TECH EEE	02	K.AMRUTHA	
B.TECH EEE	02	N.DINESH	
B.TECH EEE	02	G.BHUVANESWAR REDDY	
B.TECH EEE	02	K.PAVAN KALYAN	
B.TECH EEE	02	N.UDAY KUMAR	
B.TECH EEE	02	K.ESWAR	
B.TECH EEE	02	S.PRIYANKA	
B.TECH EEE	02	K.VENKAT	
B.TECH EEE	02	N.AJAY	
B.TECH EEE	02	A.VINAY KUMAR	

HEAD OF THE DEPARTMENT

Head of Department
ELECTRICAL & ELECTRONICS ENGINEERING
PBR Visvodaya Institute of Technology & Science
KAVALI - 524 201, SPSR Nellore (Dt) A.P.

भारत हेवी इलेक्ट्रिकल्स लिमिटेड
रामचंद्रापुरम, हैदराबाद
मानव संसाधन विकास केंद्र

BHARAT HEAVY ELECTRICALS LIMITED
RAMACHANDRAPURAM, HYDERABAD-502032
Human Resource Development Centre

Ref No: 21ENGG4079 **Date :** 02/11/2021

TO WHOMSOEVER IT MAY CONCERN

This is to certify that Mr./Ms./Mrs. K. REDDY MONICA with college id no: 19735A0225 studying in PBR VISVODHAYA INSTITUTION/ TECHNOLOGY AND SCIENCE pursuing B.E/B.Tech/MBA in ELECTRICAL AND ELECTRONICS ENGINEERING discipline had undergone project training from 19/10/2021 to 02/11/2021. The title of the project as per our records is "STUDY OF TURBO GENERATORS".

K. Sahesh
के. एच. सहेश
कार्यपालक / मा.सं. (टी डी एच)
Sr. Executive / HR - TDX
बी.एच.ई.एल. हैदराबाद BHEL, HYD-32

Project training in-charge

PARVATHAREDDY BABUL REDDY
VISVODAYA INSTITUTE OF TECHNOLOGY & SCIENCE
(Affiliated to J.N.T.U., Anantapur & Approved by AICTE, New Delhi, Accredited by NAAC 'A')
KAVALI - 524 201, S.P.S.R. Nellore Dist., A.P., India. ☎ 08626 - 243930

Date: 09/10/2021

To,
The General Manager,
BHEL,
Ramachandrapuram,
Hyderabad.

Sir,

Sub: P.B.R. Visvodaya Institute of Technology & Science – Permission for Internship for B.Tech student – Request – Regarding

It is to bring to your kind notice that, Our B.Tech. (EEE) Final year student **Ms K.Reddy Monica bearing Roll.No 19735A0225** is interested to take up internship for a period of 15 days at your organization i.e from 10.10.2021 to 25.10.2021. The internship helps her to acquaint with various functional areas of the organization, besides becoming familiar with the concepts learnt/ to be learnt in various courses.

Hence, I request you to accord permission to our of Final year B.Tech student and provide her an opportunity to pursue internship in your esteemed organization. It will be kind of you if you could provide guidance to our student and help her to gain knowledge in chosen area of specialization.

I assure you that our student will not disturb your work and maintain discipline in your organization. Kindly do the needful.

Thanking you,

Yours faithfully,

PRINCIPAL
PARVATHAREDDY BABUL REDDY
VISVODAYA INSTITUTE OF TECHNOLOGY & SCIENCE
KAVALI - 524 201, SPSR Nellore Dist., Andhra Pradesh

PERSONIFWY

TRAINING COMPLETION CERTIFICATE

THIS IS TO CERTIFY THAT

Kuraku Pavan Kalyan

participated and successfully completed the training program in
Artificial Intelligence with Python from 12th Aug, 2022 to 05th Sep, 2022

07-SEP-2022

ISSUE DATE

Coincent
Learning Drives Excellence

SIGNATURE

IMV-220903918

SOUTHREN POWER DISTRIBUSTION COMPANY OF A.P. LTD.

OPERATION SECTION KAVALI TOWN -1

CERTIFICATE OF APPRENTICE

THIS IS CERTIFIED THAT

MR. BEERAKAYALA MADHAN

OF 4th B.Tech in ELETRICAL & ELECTRONICS ENGG. At ParvathaReddy Babul Reddy Visvodaya Institute Of Technology & Science Student of bearing pin No: ***19731A0203.****As undergoing industrial training at OFFICE OF ASSISTANT ENGINEER OPERATION/APSPDCL TOWN-1 –SECTION, KAVALI. He is successfully completed his training of* ***months*** *from* ***17-08-2022 to 05-09-2022*** *and his performance during the above period his conduct and performance is satisfactory*

Asst.Executive Engineer
Operation::APSPDCL
KAVALI TOWN – I

DATE: 05-09-2022

PLACE: KAVALI

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms....P. Dhanesh.....S/O or D/O....P. Venkat rao.

Pin no.....20735A0213.....has undergone.....18.....days of training i.e,

from.....17-08-2018.....to.....05-09-2018.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.K.NITHISH KUMAR REDDY S/O or D/O.K.KRISHNA REDDY

Pin no.19731A0216.....has undergone.....18.....days of training i.e,

from..17-08-2022.....to.....05-09-2022...in APSPDCL operation section kavali rural. In the part of education. His/Her performance and conduct during this period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms A. vijay sai kumar S/O or D/O A Gopal

Pin no. 20735A0205 has undergone 18 days of training i.e,

from 17-08-2022 to 06-09-2022 in APSPDCL operation section kavali

Town-1 In the part of education. His/Her performance and conduct during this

period is Satisfactory

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms....A venu.....S/O or D/O.A.srinivasulu.....

Pin no...20735A0225.....has undergone.....18.....days of training i.e,

from..17-08-2022.....to...05-09-2022...in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....S.K.:Sandhani.....S/O or D/O...S.K.:Fakruddin

Pin no.....20735A0216.....has undergone.....18.....days of training i.e,

from.....17-08-2022.....to.....05-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.SK.SULTHAN BASHA S/O or D/O SK.KARIMULLA

Pin no.20733-A-0207 has undergone 18 days of training i.e,

from 13-08-2022 to 30-09-2022 in APSPDCL operation section kavali

Town-1 In the part of education. His/Her performance and conduct during this

period is Satisfactory

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power
Distribution Company of A.P. ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms. SK. JAKEESHARIF ....S/O or D/O. SK. KARIMULLA

Pin no. 19731A0232 .....has undergone ..... 18 .....days of training i.e,

from ..... 13-09-2022 ....to ..... 5-09-2022 ....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is ..... Satisfactory

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

POWER LINE OUR LIFE LINE

S/D

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.M.PRASAD REDDY.....S/O or D/O.M.BHASKAR REDDY

Pin no..19731A0223.....has undergone.....18.....days of training i.e,

from..17-08-2022.....to..5-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that ~~Mr~~/Ms.....D. Abhinaya.....S/O or D/O.D. Ramesh Reddy

Pin no.....19731A0212.....has undergone.....27.....days of training i.e,

from.....10/08/2022.....to.....05/09/2022.....in APSPDCL operation section kavali Town—II. In the part of education. His/Her performance and conduct during this period is.....Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....G. Sreeja.....S/O or D/O....G. kondalrao....

Pin no.....197310A0213.....has undergone.....27.....days of training i.e,

from.....10/08/2022....to.....05/09/2022..in APSPDCL operation section kavali Town—II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....K: Sangeetha.....S/O or D/O.K: Malakonda Reddy

Pin no.....19731A0420.....has undergone.....47.....days of training i.e,

from.....10/08/2022.....to.....05/09/2022...in APSPDCL operation section kavali Town—II. In the part of education. His/Her performance and conduct during this period is.....Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....Ch: Nani.....S/O or D/O....Ch: Papaiah.....

Pin no.....207335A0421.....has undergone.....27.....days of training i.e,

from.....10/08/2022....to.....05/09/2022...in APSPDCL operation section kavali

Town—II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....Sk:.Shameer.....S/O or D/O...Sk:Nagoor.Basha

Pin no.....20735A0230.....has undergone.....27.....days of training i.e,

from.....10/08/2022.....to.....05/09/2022...in APSPDCL operation section kavali

Town—II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms..శ్రీ.V.Ramachandraiah...S/O or D/Oశ్రీ:..Yedukondalu.

Pin no....211325A0212.....has undergone.....27.....days of training i.e,

from.....10/08/2022.....to.....05/09/2022...in APSPDCL operation section kavali

Town—II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms...R.Venkata Manu.....S/O or D/O..R.Tirupathaiah..

Pin no.....20735A0215.....has undergone.....27.....days of training i.e,

from.....19/08/2023.....to.....05/09/2023...in APSPDCL operation section kavali Town—II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....K. Vijaya Sai.....S/O or D/O.K. Prasannanjaneyulu

Pin no.....20735A0228.....has undergone.....27.....days of training i.e,

from.....10/08/2022.....to.....05/09/2022...in APSPDCL operation section kavali Town--II. In the part of education. His/Her performance and conduct during this period is...Good.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI TOWN--II

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ
Internship certificate

This is to certify that Mr/Ms. VALLURU LAKSHMI NARAYANA S/O or D/O VALLURU VENKATA NARAYANA

Pin no. 20735A0226 has undergone 19 days of training i.e,

from 17-08-2022 to 5-09-2022 in APSPDCL operation section kaligiri

Town . In the part of education. His/Her performance and conduct during

this period is SATISFACTORY

Asst. Executive Engineer
Distribution APSPDCL
kaligiri TOWN

Assistant Engineer
Operation : APSPDCL
KALIGIRI

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ
Internship certificate

This is to certify that Mr/Ms. SUDDULA VAMSIKRISHNA S/O or D/O SUDDULA SRINIVASULU

Pin no. 19731A0235 has undergone 19 days of training i.e,

from 17-08-2022 to 5-09-2022 in APSPDCL operation section kaligiri

Town . In the part of education. His/Her performance and conduct during this period is SATISFACTORY

Asst. Executive Engineer
Distribution APSPDCL
kaligiri TOWN

Asst. Executive Engineer
Operation APSPDCL
KALIGIRI

APSIS Solutions

INNOVATING THROUGHOUT

INTERNSHIP CERTIFICATION

This is to certify that

Kolluboina Venkatesh

has successfully completed internship program in **IoT, Robotics & Embedded Systems** from 12th Aug, 2022 to 05th Sep, 2022. During the internship, the student was found to be dedicated, hardworking and diligent.

ACADEMIC HEAD

Coincent

DIRECTOR SIGNATURE

APSIS Solutions

INNOVATING THROUGHOUT

INTERNSHIP CERTIFICATION

This is to certify that

Vasantham Pavan Kumar

has successfully completed internship program in **IoT, Robotics & Embedded Systems** from 12th Aug, 2022 to 05th Sep, 2022. During the internship, the student was found to be dedicated, hardworking and diligent.

ACADEMIC HEAD

Coincent

DIRECTOR SIGNATURE

PERSONIFWY

INTERNSHIP
CERTIFICATION

This is to certify that

K.vishnuvardhan

has successfully completed internship program in **Artificial Intelligence with Python** from 12th Aug, 2022 to 05th Sep, 2022. During the internship, the student was found to be dedicated, hardworking and diligent.

ACADEMIC HEAD

Coincent

DIRECTOR SIGNATURE

पावरग्रिड
POWERGRID

पावर ग्रिड कॉर्पोरेशन ऑफ इंडिया लिमिटेड
(भारत सरकार का उद्यम)
POWER GRID CORPORATION OF INDIA LIMITED
(A Government of India Enterprise)

Ref: SRTS-I:NLR:HRD:Industrial Training/

Date:05.09.2022

TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Shri. Sadu Tarun**, a student of 4th year B-Tech (EEE) from Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali-524201, Nellore Dist., AP, Regn.No.19731A0229, has successfully completed Industrial Training /Internship for Two weeks from 23.08.2022 to 05.09.2022 at Nellore 400kV Substation, Power Grid Corporation of India Limited, Nellore Dist.-524405, Andhra Pradesh as part of his curriculum of his course.

For Power Grid Corporation of India Limited.

5/9/22

(K.Sudhakar Rao)
General Manager
Nellore Station

R. Ramulu
DGM/SS

To

Shri.Sadu Tarun,
4th year B-Tech (EEE) Student,
Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali-524201, Nellore Dist. Andhra Pradesh.

INDUSTRIAL TRAINING TO THE EEE STUDENTS

This is to certify that **Mr Guduri Jashuva S/o Venkataiah**, a student of **PBR Visvodaya Institute of Technology and Science, Kavali**, Bearing Roll **No: 20735A0202**, has successfully completed 18 days Industrial Training Programme in **APCPDCL**, operation section, **Kanigiri**.

During the training period from 19/08/2022 to 05/09/2022 her performance and conduct is satisfactory.

Date: 05/09/2022

Place: Kanigiri Town

Asst Executive Engineer

ASST.EXECUTIVE ENGINEER
OPERATION : APSPDCL
Operation/Kanigiri KANIGIRI TOWN

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

INDUSTRIAL TRAINING TO THE EEE STUDENTS

This is to certify that **Miss Jadda Keerthi D/o Masthanaiah**, a student of **PBR Visvodaya Institute of Technology and Science, Kavali**, Bearing Roll No: **19731A0214**, has successfully completed 18 days Industrial Training Programme in **APSPDCL**, operation section, **Venkatachalam**.

During the training period from 19/08/2022 to 05/09/2022 her performance and conduct is satisfactory.

Date: 05/09/2022

Place: Venkatachalam

Asst Executive Engineer

Operation/ Venkatachalam

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms. CH. Suneel S/O or D/O. CH. Veera Swamy

Pin no. 19731A0205 has undergone 21 days of training i.e,

from 18.08.2022 to 08.09.2022 in APSPDCL operation section NAIDUPETA TOWN. In the part of education. His/Her performance and conduct during this period is Good

Assistant Engineer
Distribution APSPDCL
NAIDUPETA TOWN

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship Certificate

This is to certify that Mr/Ms. ANDRA NAGENDRA REDDY ....S/O or D/O. GURAVA REDDY .....

Pin no. 20135A0224 .....has undergone ..... 23 days .....days of training i.e,

from. 17/08/2022 .....to. 08/09/2022 .....in APSPDCL (33/11 KV) SUBSTATION operation section varikuntapadu town. In the part of education. His/Her performance and conduct during this period is ..... Satisfactory .....

Asst. Executive Engineer
Distribution APSPDCL
VARIKUNTAPADU TOWN

SOUTHERN POWER DISTRIBUTION COMPANY OF ANDHRA PRADESH Ltd

Nellore
05.09.2022

To
Dr.B. Dattatraya Sarma M.Tech,PhD
Principal
PBR VITS
KAVALI- 524201.

Sub:- APSPDCL-TRE-Sub Division-Certificate of Completion of Internship of KUCHIREDDY LIKITHA MADHAVI, Roll No.19731A0219,IV B.Tech, EEE,PBR VITS,Kavali-524201-Reg.

Ref: 1. Your Letter Dated.17-08-2022
2. Memo.No.SE/O/NLR/PO/JAO/Adm/JA-1/D.No.1505/2022 Dt.18.08.2022

This is to certify that **KUCHIREDDY LIKITHA MADHAVI** Student of PBR VITS,Kavali with Roll No.19731A0219, IV B.Tech, EEE, has completed her three weeks of internship with us, from 17th August,2022 to 5th September 2022.

As part of her internship she has done a study on "Maintenance of 33/11KV sub Stations" in Transformers Division. During her internship, she has studied 33/11 KV Power Transformers, 33&11KV Vaccum circuit breakers, 11KV Capacitor Banks, Earthing of Sub Stations and all sub-station maintenance schedules.

During her tenure with us, we found KUCHIREDDY LIKITHA MADHAVI is sincere and result oriented.

We wish **KUCHIREDDY LIKITHA MADHAVI** all the best for her future endeavours.

K Vijay Kumar Reddy
Deputy Executive Engineer
TRE Sub Division
APSPDCL
NELLORE

Southern Power
Distribution Company of A.P. Ltd

INDUSTRIAL TRAINING TO THE EEE STUDENTS

This is to certify that Miss Yallampalli Pravallika D/O Seenaiah,

a student of PBR Vishvodaya Institute of Technology and Science, Kavali, Bearing PIN NO: 19731A0243, has successfully completed 18 Days Industrial training program in APSPDCL, Operation Section, Buchi Reddy Palem.

During the Training period from 19.08.2022 to 05.09.2022 her Performance and Conduct is Satisfactory.

Date: 05.09.2022

Place: Buchi Reddy Palem

Sk. Z. Basheer 5/9/22
Asst Executive Engineer
ASSISTANT ENGINEER
OPERATION :: APSPDCL
BUCHI TOWN
Operation / Buchi Town

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

INDUSTRIAL TRAINING TO THE EEE STUDENTS

This is to certify that **Mr Dasari Gangadhar S/o Chinna Nagaiah** a student of **PBR Visvodaya Institute of Technology and Science, Kavali**, Bearing Roll **No: 19731A0210**, has successfully completed 18 days Industrial Training Programme in **APSPDCL**, operation section, **Duttalur**.

During the training period from 19/08/2022 to 05/09/2022 her performance and conduct is satisfactory.

Date: 05/09/2022

Place: Duttalur

Asst Executive Engineer

Assistant Engineer
Operation, APSPDCL
DUTTALURU

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/~~Ms~~.M:RAVI TEJA...S/O or ~~D/O~~.M:RAMESH

Pin no..19731A0222...has undergone.....18.....days of training i.e,

from...17-08-22...to...05-09-22...in APSPDCL operation section kaligiri

Town. In the part of education. His/Her performance and conduct during this period is.....05-09-2022 [SatisFactory]

Assistant Engineer
Operation SAP SD
APSPDCL

Asst. Executive Engineer
Distribution APSPDCL
KALIGIRI

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms. Ravuri Meghana S/O or D/O. Srinivasulu

Roll no. 19731A02254 has undergone 25 days of training i.e,

from 17.08.2022 to 02.09.2022 in APSPDCL operation section Damaramadugu. In the part of education. His/Her performance and conduct during this period is. Satisfactory

Asst. Executive Engineer
APSPDCL
Buchireddypalem

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms DARA. MAHITH S/O or D/O JACOB

Roll no 19731A02D8 has undergone 16 days of training i.e,

from 17.08.2022 to 05.09.2022 in APSPDCL operation section Damaramadugu. In the part of education. His/Her performance and conduct during this period is Satisfactory.

Asst. Executive Engineer
APSPDCL
Buchireddypalem

LANARSY
building excellence...innovatively

To whom it may concern

This is to certify that Mis.**Byrisetti Saritha,** D/o. **Byrisetti Bhasker Rao,** bearing Roll no:- **19731A0204** who is pursuing her B.Tech from PBR Visvodaya Institute Of Technology and Science, Kavali, has successfully completed her internship programme/training at 220/66/11Kv Substation in Kudligi from 20-08-2022 to 05-09-2022.

During the training period, we found her sincere, hardworking and she worked well as part of team during her tenure.

Lanarsy Infra Limited

LANARSY INFRA LIMITED KUDLIGI

Authorized Signatory
Substation Incharge.
Substation and O&M Division.
Kudligi.

LANARSY
building excellence innovatively

To whom it may concern

This is to certify that Mis.**Adigentla Sujitha,** D/o. **Adigentla Subbaiah**, bearing Roll no:- **19731A0201** who is pursuing her B.Tech from PBR Visvodaya Institute Of Technology and Science, Kavali, has successfully completed her internship programme/training at 220/66/11Kv Substation in Kudligi from 20-08-2022 to 05-09-2022

During the training period, we found her sincere, hardworking and she worked well as part of team during her tenure.

Lanarsy Infra Limited

LANARSY INFRA LIMITED KUDLIGI

Authorized Signatory
Substation Incharge.
Substation and O&M Division.
Kudligi.

CENTRAL POWER DISTRIBUTION CORPORATION OF AP LIMITED

CERTIFICATE

This is to certify that Sri. **Boina Praveen Kumar S/o Sri B.Chinna Malakondaiah** a student of **PBR Visvodaya Institute of Technology & Science, Kavali** Bearing Roll No: **20735A0206** has successfully completed B.Tech Industrial Internship in **APCPDCL, OPERATION, DIVISION OFFICE, KANDUKUR** during the period from **19.08.2022 to 08.09.2022.**

His/ Her performance during the training is Satisfactory.

Date:

Place: Kandukur

EXECUTIVE ENGINEER
OPERATION :: KANDUKUR

CENTRAL POWER DISTRIBUTION CORPORATION OF AP LIMITED

CERTIFICATE

This is to certify that **Sri. SUNKARA RENUKA D/o Sri S.NARASIMHARAO** a student of PBR Visvodaya Institute of Technology & Science, Kavali Bearing Roll No: **19731A0236** has successfully completed B.Tech Industrial Internship Program **OPERATION, DIVISION OFFICE, KANDUKUR** during the period from **19.08.2022 to 08.09.2022**.

నీదో మీ సేవలో...

His/ Her performance during the training is Satisfactory.

Date: 8.9.2022

Place: Kandukur

EXECUTIVE ENGINEER
OPERATION :: KANDUKUR

CENTRAL POWER DISTRIBUTION CORPORATION OF AP LIMITED

CERTIFICATE

This is to certify that **Sri. KOLLABATHINA AMULYA D/o Sri K.PANDU** a student of **PBR Visvodaya Institute of Technology & Science, Kavali** Bearing Roll No: **19731A0217** has successfully completed B.Tech Industrial Internship Program in **OPERATION, DIVISION OFFICE, KANDUKUR** during the period from **19.08.2022 to 08.09.2022**.

నాదో మీ సేవలో...

His/ Her performance during the training is Satisfactory.

Date: 9-9-2022

Place: Kandukur

EXECUTIVE ENGINEER
OPERATION :: KANDUKUR

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	PARA UMESH CHAND
2	**Roll No.**	: 19731A0253
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	ERRAJONNALA RAJU
2	**Roll No.**	: 16731A0215
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	VISHITHA DARA
2	**Roll No.**	: 19731A0242
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	VAKA PRAVALIKA
2	**Roll No.**	: 19731A0240
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	VAJJA SANDEEP
2	**Roll No.**	: 19731A0239
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	THUPILI PRAVEEN
2	**Roll No.**	: 19731A0238
3	**Class studying**	: 4rd year, B.Tech(EEE)
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Thermal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

12/9/22

Executive Engineer
EM & MRT, SDSTPS

ANDHRA PRADESH POWER GENERATION CORPORATION LTD
SRI DAMODARAM SANJEEVAIAH THERMAL POWER STATION
Nelatur(village),S.P.S.R.Nellore(Dst),Andhra Pradesh.

TRAINING CERTIFICATE

1	**Name of the Student**	: SHAIK YASIN
2	**Roll No.**	: 19731A0233
3	**Class studying**	: 4rd year, B.Tech
4	**College from which deputed**	: Parvathareddy Babul Reddy Visvodaya Institute of Technology & Science, Kavali
5	**Place/Places of Training**	: 2X800 MW ,Sri Damodaram Sanjeevaiah Themal Power Station, Nelatur, Nellore.
6	**Period of Training undergone**	: 22-08-2022 TO 12-09-2022
7	**Attendance**	: Regular
8	**Particulars of Training undergone**	: Internship Training of 2X800 MW On Electrical Systems 400KV Switchyard, Transformers, HT/LT Switch Gear, Turbo Generator, ESP, Motors, Boiler, WTP & CHP.
9	**Performance of the Trainee**	: Good
10A	**Conduct of the Trainee**	: Good
11	**CE's office reference in which orders are accorded**	: Proceedings Lr.No.CE(O&M)/ SDSTPS /GM(HR)/PO/SA / F.NO.25 /D.NO.473/22, Dt.22.08.22

12/9/22

Executive Engineer
EM & MRT, SDSTPS

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms. R. VASWANTH ..... S/O or D/O. R. BALAKRISHNA

Pin no. 207350219 ..... has undergone ... 15 DAYS ..... days of training i.e,

from ..17-08-2022.... to ..... 5-09-2022 ... in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is ..... Satisfactory .....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....R. Mahendra Simha S/O or D/O...R. Ramesh.....

Pin no.....20735A0229.....has undergone.....18.....days of training i.e,

from..17-8-2022.....to..5-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....T. Ramakrishna.....S/O or D/O.....T. Seenaiah.....

Pin no.....20735A0217.....has undergone.....days of training i.e,

from.....17-08-2022.....to.....05-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.A.VENKATESH.....S/O or D/O..A..MURALI...

Pin no.20735A0201...has undergone.....18.....days of training i.e,

from...13-08-2022.....to.....31-08-2022...in APSPDCL operation section kavali rural. In the part of education. His/Her performance and conduct during this period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms..E.SRINADH.....S/O or D/O.E.MOHANRAO....

Pin no.207350D204.....has undergone.....18.....days of training i.e,

from..17-08-2022.....to.....5-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....P. Venkateswarlu.....S/O or D/O.....P. Srinu.....

Pin no.....20735A0214.....has undergone.....18.....days of training i.e,

from.....17-08-2022.....to.....05-09-2022.....in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

POWER LINE OUR LIFE LINE

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

విద్యుత్ శక్తి మన జీవన శ్వాస

Internship certificate

This is to certify that Mr/Ms.....S.V. Satwika.....S/O or D/O.....S.V. Ratnam.....

Pin no.....20735A0206.....has undergone.....18.....days of training i.e,

from...17-08-2022.....to...7-09-2022...in APSPDCL operation section kavali

rural. In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI rural

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms. M.IMMANUEL .....S/O or D/O. M.VENKATESWARLU

Pin no. 20735A0203 .....has undergone .....18..... days of training i.e,

from ...17-08-2022..... to ....5-09-2022.... in APSPDCL operation section kavali

Town-1 In the part of education. His/Her performance and conduct during this

period is Satisfactory .....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms..N:.Siva kavitha.....S/O or D/O..N:..Malyadri.

Pin no...197311A0226.....has undergone.....18.....days of training i.e,

from...17-.08-.2022.....to.....7-.09-.2022...in APSPDCL operation section kavali

Town-1 In the part of education. His/Her performance and conduct during this

period is.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms.....S/O or D/O.....

Pin no.....has undergone.....18.....days of training i.e,

from.....17-08-2022.....to.....5-09-2022.....in APSPDCL operation section kavali

Town -1 In the part of education. His/Her performance and conduct during this period is.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms....K. Anusha.....S/O or D/O....K. Sudhakar.....

Pin no.....19731A02147.....has undergone.....18.....days of training i.e,

from....17-08-2022.....to.....5-09-2022.....in APSPDCL operation section kavali

Town-1 In the part of education. His/Her performance and conduct during this

period is.....Satisfactory.....

Asst. Executive Engineer
Distribution APSPDCL
KAVALI Town - 1

Southern Power AP

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/Ms...K. AMRUTHA...s/o or D/o K. Venkateswarlu

Pin no.207735A0221 has undergone.....18.....days of training i.e,

from...19..08..2022..to...5..09..2022....in APSPDCL operation section varikuntapadu. In the part of education. His/Her performance and conduct during this period is.....Good.....

Bhask
Assistant Engineer
Operation APSPDCL
Podalakuru

Assistant Engineer
Operation APSPDCL
Podalakuru

Southern Power
Distribution Company of A.P. Ltd
దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Southern Power AP

Internship certificate

This is to certify that Mr/Ms..N. DINESH.....S/O or D/O..Venkateswarlu

Pin no.19731A0224..has undergone.....days of training i.e,

from..12-08-2022.to..08-09-2022.in APSPDCL operation section varikuntapadu. In the part of education. His/Her performance and conduct during this period is.....Good.....

Assistant Engineer
Operation, APSPDCL
Podalakuru

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Southern Power AP

Internship certificate

Internship certificate This is to certify that Mr/Ms G. BHUVANESWAR REDDY S/O or ~~D/O~~ SRINIVASA REDDY Pin no 207735A0231 has undergone 27 days days of training i.e, from 12-08-2022 to 08-9-2023 in APSPDCL 33/11KV operation section Podalakuru. In the part of education. His/Her performance and conduct during this period is Good Assistant Engineer Operation, APSPDCL Podalakuru

Bhask

Assistant Engineer
Operation, APSPDCL
Podalakuru

PERSONIFWY

INTERNSHIP
CERTIFICATION

This is to certify that

Nasina.udaykumar

has successfully completed internship program in **Artificial Intelligence with Python** from 12th Aug, 2022 to 05th Sep, 2022. During the internship, the student was found to be dedicated, hardworking and diligent.

ACADEMIC HEAD

Coincent

DIRECTOR SIGNATURE

SOUTHERN POWER DISTRIBUTION COMPANY OF ANDHRA PRADESH. Ltd

Sub - APSPDCL-33/11 KV SUB-STATION TRAINING Certificate of Internship **KAPPALA ESWAR** Roll No. **19731A0255** .IV B.Tech. EEE. PBR VIT'S, Kavali-524201

This is to the **KAPPALA ESWAR** Student of **PBR VITS** ,with **Roll No-19731A0255 IV B.TECH. EEE**. has completed his three weeks Of internship with us, from 17th August,2022 to 5th September ,2022

As pad of his internship he has done a study on •Maintenance of 33/11KV sub Stations* in Transformers Division. During his internship. He has studied 33/11 KV Power Transformer.Sub - Station and all sub-station maintenance

During his training with us. we found **KAPPALA ESWAR** is sincere & result oriented

A. NIRANJAN
ASST.EXECUTIVE ENGINEER
A.S PETA
524304

Assistant Engineer
Operation, APSPDCL
A. S. PET

CENTRAL POWER

APCPDCL Distribution Corporation of A.P.Ltd.

CERTIFICATE

This is to certify that **Miss S.Priyanka** bearing Rollno.**19731A0230** studying B.Tech, III year(EEE) "from PBR Visvodaya Institute Technology And Science Engineering College, Kavali, Nellore district"has undergone internship training in 33KV/11kv Substation, Adavi nakkala, Nuzvid division from "**17-08-2022** to **04-09-2022** and successfully completed."

During the above period her conduct is satisfactory

Assistant engineer

33/11 KV Sub Station, Adivinekkalam,

APCPDCL.

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/~~Ms~~.V.:VENKAT.....S/O or ~~D/O~~.V.:SRINIVASULU

Pin no.197310241....has undergone.....18.....days of training i.e,

from..17.-.08.-.22.to..05.-.09.-.22.in APSPDCL operation section kaligiri

Town. In the part of education. His/Her performance and conduct during this period is.....

Asst. Executive Engineer
Distribution APSPDCL
KALIGIRI

Assistant Engineer
Operation APSPDCL
KALIGIRI

Southern Power
Distribution Company of A.P. Ltd

దక్షిణ ప్రాంత విద్యుత్ పంపిణీ సంస్థ

Internship certificate

This is to certify that Mr/~~Ms~~..N.AJAY.....S/O or ~~D/O~~..N.VASU.....

Pin no...197310225....has undergone.....18.....days of training i.e,

from..17-08-22..to..05-09-22..in APSPDCL operation section kaligiri

Town. In the part of education. His/Her performance and conduct during this period is.....

Asst. Executive Engineer
Distribution APSPDCL
KALIGIRI

Assistant Engineer
Operation : APSPDCL
KALIGIRI

SOUTHREN POWER DISTRIBUSTION COMPANY OF A.P. LTD.

OPERATION SECTION KAVALI TOWN -1

CERTIFICATE OF APPRENTICE

THIS IS CERTIFIED THAT

MR. ATMAKURU VINAY KUMAR

OF 4th B.Tech in ELETRICAL & ELECTRONICS ENGG. At ParvathaReddy Babul Reddy Visvodaya Institute Of Technology & Science Student of bearing pin No: ***19731A0202.*** *As undergoing industrial training at OFFICE OF ASSISTANT ENGINEER OPERATION/APSPDCL TOWN-1 –SECTION, KAVALI. He is successfully completed his training of* ***months*** *from* ***17-08-2022 to 05-09-2022*** *and his performance during the above period his conduct and performance is satisfactory*

DATE: 05-09-2022

PLACE: KAVALI

Asst.Executive Engineer

Operation::APSPDCL

MIND TREE - 4.0 LKS

Sno	Roll No	Candidate Name	Gender	College	Departmen
1	18731A0506	BOGGARAPU LAKSHMI SAI RAMYA	FEMALE	VITS	CSE
2	18731A0541	VEMA LAKSHMI KIRTHNA SREEJA	FEMALE	VITS	CSE
3	18731A0560	PASUPULETI CHINNA VENGABABU	MALE	VITS	CSE
4	18731A0567	SHAIK AKHILA	FEMALE	VITS	CSE
5	18731A0575	VANTERU HEMALATHA	FEMALE	VITS	CSE
6	18731A0576	VISWANADHUNI LAKSHMI SARAYU	FEMALE	VITS	CSE
7	18731A05B7	KONDAPALLI SRAVAN	M	VITS	CSE
8	18731A05F0	SHAIK IMRAN	MALE	VITS	CSE

WIPRO - 4.0 LKS

Sno	Roll No	Candidate Name	Gender	College	Departmen
1	18731A0504	AMBATI VENKATA SUSHMA	FEMALE	VITS	CSE
2	18731A0510	GADAMSETTY DEVAHARSHINI	FEMALE	VITS	CSE
3	18731A0511	GADDAM AKHILA	FEMALE	VITS	CSE
4	18731A0517	KONANKI KEERAVANI	FEMALE	VITS	CSE
5	18731A0521	MANGILIPUDI KEERTHI REDDY	FEMALE	VITS	CSE
6	18731A0526	NAGA GREESHMA REDDY	FEMALE	VITS	CSE
7	18731A0529	PALAPARTHI KOUSIK	MALE	VITS	CSE
8	18731A0530	PULIVARTHI SAI JYOTHSNA	FEMALE	VITS	CSE
9	18731A0531	PUSALA HEMANTH	MALE	VITS	CSE
10	18731A0535	SITHA THARUN SAI	MALE	VITS	CSE
11	18731A0536	SOMISETTY VEENA VANI MEGHANA	FEMALE	VITS	CSE
12	18731A0538	VAKA MANASA	FEMALE	VITS	CSE
13	18731A0539	VALIVARTHI RAMU	MALE	VITS	CSE
14	18731A0540	VALLETI SIREESHA	FEMALE	VITS	CSE
15	18731A0543	BINCY SREENIVASA CHOWDARI PONDURI	MALE	VITS	CSE
16	18731A0545	CHITTABATHINA SOWMYAPRIYA	FEMALE	VITS	CSE
17	18731A0551	GUDA SIVANI	FEMALE	VITS	CSE
18	18731A0553	KASIREDDY ABHINANDANA REDDY	MALE	VITS	CSE
19	18731A0554	MADHIRI SANDEEP	MALE	VITS	CSE
20	18731A0556	NANDYALA HARINATHA REDDY	MALE	VITS	CSE
21	18731A0557	NELLORE MANOGNA	FEMALE	VITS	CSE
22	18731A0562	PODA APARNA	FEMALE	VITS	CSE
23	18731A0565	RASAPUTRA SIVANI SINGH (non-plmt)	FEMALE	VITS	CSE
24	18731A0566	SANA JHANSI	FEMALE	VITS	CSE
25	18731A0567	SHAIK AKHILA	FEMALE	VITS	CSE
26	18731A0569	SURAGANI MUKESH	MALE	VITS	CSE
27	18731A0570	SYED AFRID	MALE	VITS	CSE
28	18731A0571	TAMMINENI SRILATA SIVANI	FEMALE	VITS	CSE
29	18731A0574	VALLABHANENI MANOJ KUMAR	MALE	VITS	CSE
30	18731A0575	VANTERU HEMALATHA	FEMALE	VITS	CSE
31	18731A0576	VISWANADHUNI LAKSHMI SARAYU	FEMALE	VITS	CSE
32	18731A0587	NANNURI MANJULA	FEMALE	VITS	CSE
33	18731A0590	KUNI SAI SUMANTH	MALE	VITS	CSE
34	18731A0597	PUSALA DHARANI	FEMALE	VITS	CSE
35	18731A05B7	KONDAPALLI SRAVAN	MALE	VITS	CSE
36	18731A05C1	MORLA VENKATA MAHESH	MALE	VITS	CSE
37	18731A05D0	ADAPALA SUSHMA	FEMALE	VITS	CSE
38	18731A05D4	CHENNAREDDY MADHAVA REDDY	MALE	VITS	CSE
39	18731A05F2	SUNKU VENKATA SAI RIKITHA	FEMALE	VITS	CSE
40	18731A05F4	THUMMALA LAKSHMI NEHA CHOWDARY(Non- Plmt)	FEMALE	VITS	CSE

1	18731A0522	MANNEM LIKITHA	FEMALE	VITS	CSE
2	18731A0599	SHAIK KOUSER	FEMALE	VITS	CSE
3	18731A05A6	CHENI KEERTHI	FEMALE	VITS	CSE
4	18731A05C0	MALLELA HEMASRI	FEMALE	VITS	CSE
5	18731A05E8	PONGULURU NIKHILESH REDDY	MALE	VITS	CSE
6	18731A0593	PANDI MADAN KUMAR	MALE	VITS	CSE
7	18731A0564	RACHAPUTI AJITHA	FEMALE	VITS	CSE
8	18731A05E1	NALLURU JYOTHI MANASWINI	FEMALE	VITS	CSE
9	18731A05E4	NELAPATI SRIDHAR	MALE	VITS	CSE
10	18731A0544	CHALUVADI SUBHAVIGNA	FEMALE	VITS	CSE

IBM - 4.5 LKS

Sno	Roll No	Candidate Name	Gender	College	Departmen
1	18731A0566	SANA JHANSI	F	VITS	CSE

PERSISTANT - 4.7 LKS

Sno	Roll No	Candidate Name	Gender	College	Departmen
1	18731A0506	BOGGARAPU LAKSHMI SAI RAMYA	FEMALE	VITS	CSE
2	18731A0507	CHEEDELLA SRI SAI VAISHNAVI	FEMALE	VITS	CSE
3	18731A0510	GADAMSETTY DEVAHARSHINI	FEMALE	VITS	CSE
4	18731A0514	KANDLAGUNTA MURALI KRISHNA	MALE	VITS	CSE
5	18731A0517	KONANKI KEERAVANI	FEMALE	VITS	CSE
6	18731A0521	MANGILIPUDI KEERTHI REDDY	FEMALE	VITS	CSE
7	18731A0528	NUTHALAPATI LAVANYA	FEMALE	VITS	CSE
8	18731A0529	PALAPARTHI KOUSIK	MALE	VITS	CSE
9	18731A0530	PULIVARTHI SAI JYOTHSNA	FEMALE	VITS	CSE
10	18731A0531	PUSALA HEMANTH	MALE	VITS	CSE
11	18731A0532	RAMALA HEMA SAHITHI	FEMALE	VITS	CSE
12	18731A0535	SITHA THARUN SAI	MALE	VITS	CSE
13	18731A0536	SOMISETTY VEENA VANI MEGHANA	FEMALE	VITS	CSE
14	18731A0553	KASIREDDY ABHINANDANA REDDY	MALE	VITS	CSE
15	18731A0554	MADHIRI SANDEEP	MALE	VITS	CSE
16	18731A0563	PUNURU LAKSHMI NARAYANA REDDY	MALE	VITS	CSE
17	18731A0567	SHAIK AKHILA	FEMALE	VITS	CSE
18	18731A0569	SURAGANI MUKESH	MALE	VITS	CSE
19	18731A0574	VALLABHANENI MANOJ KUMAR	MALE	VITS	CSE
20	18731A0581	BASAM BHANU PRAKASH	MALE	VITS	CSE
21	18731A0590	KUNI SAI SUMANTH	MALE	VITS	CSE
22	18731A0598	PUTTU SAI PREETHAM	MALE	VITS	CSE
23	18731A05A8	DAGGUMATI RAVIMADHUR	MALE	VITS	CSE
24	18731A05F0	SHAIK IMRAN	MALE	VITS	CSE
25	18731A05G5	GURRAM VENKATA RAMANAIAH	MALE	VITS	CSE

HEXAWARE - 4.0 LKS

Sno	Roll No	Candidate Name	Gender	College	Departmen
1	18731A0522	MANNEM LIKITHA	FEMALE	VITS	CSE
2	18731A0594	PASUPULETI VENGAMA NAIDU	MALE	VITS	CSE

DXC TECHNOLOGIES - 4.0 LKS

Sno	Roll No	Candidate Name	Gender	College
1	18731A0501	ADIMULAM NAGA LAKSHMI PRIYANKA	F	VITS
2	18731A0503	AMARA VENKATA SAI MARUTHI SWAMY SWAROOP	M	VITS
3	18731A0506	BOGGARAPU LAKSHMI SAI RAMYA	F	VITS
4	18731A0507	CHEEDELLA SRI SAI VAISHNAVI	F	VITS
5	18731A0508	CHEEDELLA VISHNU PRANATHI	F	VITS
6	18731A0510	GADAMSETTY DEVAHARSHINI	F	VITS
7	18731A0514	KANDLAGUNTA MURALI KRISHNA	M	VITS
8	18731A0517	KONANKI KEERAVANI	F	VITS
9	18731A0518	KONCHA SARITHA	F	VITS
10	18731A0519	MADDIREDDY LAKSHMI DEEPIKA	F	VITS
11	18731A0520	MAMILLAPALLI VINOD	M	VITS
12	18731A0521	MANGILIPUDI KEERTHI REDDY	F	VITS
13	18731A0524	MANUBOTHU VAISHNAVI	F	VITS
14	18731A0528	NUTHALAPATI LAVANYA	F	VITS
15	18731A0529	PALAPARTHI KOUSIK	M	VITS
16	18731A0532	RAMALA HEMA SAHITHI	F	VITS
17	18731A0538	VAKA MANASA	F	VITS
18	18731A0539	VALIVARTHI RAMU	M	VITS
19	18731A0540	VALLETI SIREESHA	F	VITS
20	18731A0541	VEMA LAKSHMI KIRTHNA SREEJA	F	VITS
21	18731A0543	BINCY SREENIVASA CHOWDARI PONDURI	M	VITS
22	18731A0545	CHITTABATHINA SOWMYAPRIYA	F	VITS
23	18731A0550	GRANDHI VENKATA KISHORE	M	VITS
24	18731A0553	KASIREDDY ABHINANDANA REDDY	M	VITS
25	18731A0557	NELLORE MANOGNA	F	VITS
26	18731A0560	PASUPULETI CHINNA VENGABABU	M	VITS
27	18731A0563	PUNURU LAKSHMI NARAYANA REDDY	M	VITS
28	18731A0567	SHAIK AKHILA	F	VITS
29	18731A0570	SYED AFRID	M	VITS
30	18731A0571	TAMMINENI SRILATA SIVANI	F	VITS
31	18731A0572	THALAPANENI JITHIN CHOWDARY	M	VITS
32	18731A0574	VALLABHANENI MANOJ KUMAR	M	VITS
33	18731A0581	BASAM BHANU PRAKASH	M	VITS
34	18731A0584	GADDIRALA THARUN MADHAN	M	VITS
35	18731A0586	INAKOLLU KOTESWARA RAO	M	VITS
36	18731A0589	KODURU JATHISHA REDDY	F	VITS
37	18731A0590	KUNI SAI SUMANTH	M	VITS
38	18731A0595	PERUGANGA VENNELA	F	VITS
39	18731A0596	PERURI LAKSHMI VINUTHA	F	VITS
40	18731A0597	PUSALA DHARANI	F	VITS
41	18731A0598	PUTTU SAI PREETHAM	M	VITS
42	18731A05A8	DAGGUMATI RAVIMADHUR	M	VITS
43	18731A05B4	GUNTAMADUGU BHAVYA	F	VITS
44	18731A05B9	MALISETTY AMRUTHA PRIYA	F	VITS
45	18731A05F0	SHAIK IMRAN	M	VITS
46	18731A05F7	JALADANKI BLESSY EVELYN	F	VITS
47	18731A05G5	GURRAM VENKATA RAMANAIAH	M	VITS
48	19735A0501	BANDI MANOJA	F	VITS

Persistent

Reference: Persistent/Academic Intern/1613966/0.2

Internship Offer Letter
Confidential

Feb 02, 2022

Mr Mukesh Suragani
Chevurivari thota
Vaikuntha puram
Nellore 524201

Dear Mukesh,

Subject:**Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as **an Academic Intern** at grade **0.2** with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

All terms and conditions in this document, read with any other document specifically referred herein and incorporated hereto by such reference, collectively shall constitute the entire understanding between the Academic Intern and the Company.

Company does not assure you or commit (a) any extension of this internship beyond the period stipulated under this letter and/or offer you employment with Company and/or absorb you as an employee of the Company in future. Unless otherwise specifically agreed in writing by Company, there shall be no employee-employer relationship between you and Company.

1. Working days
Normal working days for Company are Monday through Friday. Company observes Sunday as a compulsory weekly off and Saturday as the other weekly off day. The normal working hours are forty five hours per week.

2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

3.Termination of Internship

The internship can be terminated with one week notice or stipend (if you are eligible for stipend under this letter), in lieu of the notice period on either side.

The Company can terminate your internship without any notice period in case the internship is terminated on grounds of:

i. Breach of confidentiality or IP related obligations
ii. Violation of law
iii. Gross Misconduct
iv. Material breach of Company policy.

In such event, the Company will not be liable to pay stipend (if payment is otherwise stipulated in this letter) in lieu of notice period.

In case the last day of your internship falls on a non-working day, your last day of internship shall be the immediate previous working day.

The internship period can be terminated by whatsoever reasons by either party by giving one week notice period.

4. Dispute Resolution

In case of any dispute or disagreement in relation to the terms of this offer or matters connected thereto, you agree to negotiate in good faith to resolve such dispute or disagreement. In case you and Company fail to settle the dispute/ disagreement amicably, the same may be exclusively referred to arbitration in accordance with the provisions of Arbitration and Conciliation Act, 1996 at Pune. Each party shall bear its own costs for arbitration.

Please contact **Rajeshwari Joshi** (Ph. No.**020-66965038**) on the date of joining. We request you to report at 9 am at the address mentioned below for completion of joining formalities.

Pune
Rigveda-Yajurveda-Samaveda-Atharvaveda Plot No. 39, Phase I, Rajiv Gandhi Information Technology Park,Hinjawadi,Pune, Maharashtra, India 411057.

5. Documents required at the time of joining

At the time of joining, the following original certificates/documents along with one photocopy should be furnished.Original certificates/documents will be returned to you after verification.

Sr. No	Description
1	Certificates of educational qualification - SSC (10th Equivalent), School leaving, HSC (12th equivalent).
2	Certificate of Graduation/Post Graduation and Mark Sheets
3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

We welcome you to the Persistent family and look forward to a mutually fulfilling association.

Yours sincerely,
For Persistent Systems Ltd

Kalpana Kudlingar
Head - Campus Talent Acquisition

Acceptance of the offer

I have read and understood all the terms and conditions contained in this letter and agree to abide by the same. I am signing this letter as a token of me having accepted the offer and the terms and conditions set out in this letter.

Also, I hereby declare that nothing apart from the above mentioned clauses have been committed to me during the selection process.

I will join the Company on the date communicated to me separately.

Date: **Signature:**
Name:

Persistent Systems Limited, Bhageerath, 402, Senapati Bapat Road, Pune 411016 | Tel: +91 (20) 670 30000 | Fax: +91 (20) 6703 009
CIN – L72300PN1990PLC056696
Persistent Systems Inc., 2055 Laurelwood Rd., Suite 210 Santa Clara, CA 95054 USA | Tel: +1 (408) 216 7010
Persistent Systems France SAS, 1 rue Hector Berlioz, 38600 Fontaine, France | Tel: +33 (0) 4 76 53 35 80

Offer Letter Attachments

Response

Accept the offer

Reference: Persistent/Academic Intern/1615211/0.2

Internship Offer Letter
Confidential

Feb 02, 2022

Mr Kasireddy Abhinandana Reddy
D NO : 115, Vinayaka colony, musunuru (Village), kavali, Nellore (District)
nellore 524201

Dear Kasireddy,

Subject: **Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as **an Academic Intern** at grade **0.2** with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

All terms and conditions in this document, read with any other document specifically referred herein and incorporated hereto by such reference, collectively shall constitute the entire understanding between the Academic Intern and the Company.

Company does not assure you or commit (a) any extension of this internship beyond the period stipulated under this letter and/or offer you employment with Company and/or absorb you as an employee of the Company in future. Unless otherwise specifically agreed in writing by Company, there shall be no employee-employer relationship between you and Company.

1. Working days
Normal working days for Company are Monday through Friday. Company observes Sunday as a compulsory weekly off and Saturday as the other weekly off day. The normal working hours are forty five hours per week.

2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

3.Termination of Internship
The internship can be terminated with one week notice or stipend (if you are eligible for stipend under this letter), in lieu of the notice period on either side.

The Company can terminate your internship without any notice period in case the internship is terminated on grounds of:
i. Breach of confidentiality or IP related obligations
ii. Violation of law
iii. Gross Misconduct
iv. Material breach of Company policy.

In such event, the Company will not be liable to pay stipend (if payment is otherwise stipulated in this letter) in lieu of notice period.

In case the last day of your internship falls on a non-working day, your last day of internship shall be the immediate previous working day.

The internship period can be terminated by whatsoever reasons by either party by giving one week notice period.

4. Dispute Resolution
In case of any dispute or disagreement in relation to the terms of this offer or matters connected thereto, you agree to negotiate in good faith to resolve such dispute or disagreement. In case you and Company fail to settle the dispute/ disagreement amicably, the same may be exclusively referred to arbitration in accordance with the provisions of Arbitration and Conciliation Act, 1996 at Pune. Each party shall bear its own costs for arbitration.

Please contact **Rajeshwari Joshi** (Ph. No.**020-66965038**) on the date of joining. We request you to report at 9 am at the address mentioned below for completion of joining formalities.

Pune
Rigveda-Yajurveda-Samaveda-Atharvaveda Plot No. 39, Phase I, Rajiv Gandhi Information Technology Park,Hinjawadi,Pune, Maharashtr
India 411057.

5. Documents required at the time of joining
At the time of joining, the following original certificates/documents along with one photocopy should be furnished.Original certificates/documents will be returned to you after verification.

Sr. No	Description
1	Certificates of educational qualification - SSC (10th Equivalent), School leaving, HSC (12th equivalent).
2	Certificate of Graduation/Post Graduation and Mark Sheets
3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

We welcome you to the Persistent family and look forward to a mutually fulfilling association.

Yours sincerely,
For Persistent Systems Ltd

Kalpana Kudlingar
Head - Campus Talent Acquisition

Acceptance of the offer

I have read and understood all the terms and conditions contained in this letter and agree to abide by the same. I am signing this letter as a token of me having accepted the offer and the terms and conditions set out in this letter.

Also, I hereby declare that nothing apart from the above mentioned clauses have been committed to me during the selection process.

I will join the Company on the date communicated to me separately.

Date:

Signature:
Name:

1

Offer Letter Body

Persistent

Reference: Persistent/Academic Intern/1614925/0.2

Internship Offer Letter
Confidential

Jan 27, 2022

Mr Manoj Kumar Vallabhaneni
Janthapet south 1st line,D No:-10-30-6E/3/H,kavali
kavali 524201

Dear Manoj Kumar,

Subject:**Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as **an Academic Intern** at grade **0.2** with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

All terms and conditions in this document, read with any other document specifically referred herein and incorporated hereto by such reference, collectively shall constitute the entire understanding between the Academic Intern and the Company.

Company does not assure you or commit (a) any extension of this internship beyond the period stipulated under this letter and/or offer you employment with Company and/or absorb you as an employee of the Company in future. Unless otherwise specifically agreed in writing by Company, there shall be no employee-employer relationship between you and Company.

1. Working days
Normal working days for Company are Monday through Friday. Company observes Sunday as a compulsory weekly off and Saturday as the other weekly off day. The normal working hours are forty five hours per week.

2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

3.Termination of Internship

The internship can be terminated with one week notice or stipend (if you are eligible for stipend under this letter), in lieu of the notice period on either side.

The Company can terminate your internship without any notice period in case the internship is terminated on grounds of:
i. Breach of confidentiality or IP related obligations
ii. Violation of law
iii. Gross Misconduct
iv. Material breach of Company policy.

In such event, the Company will not be liable to pay stipend (if payment is otherwise stipulated in this letter) in lieu of notice period.

In case the last day of your internship falls on a non-working day, your last day of internship shall be the immediate previous working day.

The internship period can be terminated by whatsoever reasons by either party by giving one week notice period.

4. Dispute Resolution

In case of any dispute or disagreement in relation to the terms of this offer or matters connected thereto, you agree to negotiate in good faith to resolve such dispute or disagreement. In case you and Company fail to settle the dispute/ disagreement amicably, the same may be exclusively referred to arbitration in accordance with the provisions of Arbitration and Conciliation Act, 1996 at Pune. Each party shall bear its own costs for arbitration.

Please contact **Rajeshwari Joshi** (Ph. No.**020-66965038)** on the date of joining. We request you to report at 9 am at the address mentioned below for completion of joining formalities.

Pune
Rigveda-Yajurveda-Samaveda-Atharvaveda Plot No. 39, Phase I, Rajiv Gandhi Information Technology Park,Hinjawadi,Pune, Maharashtra, India 411057.

5. Documents required at the time of joining

At the time of joining, the following original certificates/documents along with one photocopy should be furnished.Original certificates/documents will be returned to you after verification.

Sr. No	Description
1	Certificates of educational qualification - SSC (10th Equivalent), School leaving, HSC (12th equivalent).
2	Certificate of Graduation/Post Graduation and Mark Sheets
3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

We welcome you to the Persistent family and look forward to a mutually fulfilling association.

Yours sincerely,
For Persistent Systems Ltd

Kalpana Kudlingar
Head - Campus Talent Acquisition

Acceptance of the offer

I have read and understood all the terms and conditions contained in this letter and agree to abide by the same. I am signing this letter as a token of me having accepted the offer and the terms and conditions set out in this letter.

Also, I hereby declare that nothing apart from the above mentioned clauses have been committed to me during the selection process.

I will join the Company on the date communicated to me separately.

Date: **Signature:**
Name:

Offer Letter Attachments

Response

Accept the offer

1

Offer Letter Body

Persistent

Reference: Persistent/Academic Intern/1637534/0.2

Internship Offer Letter
Confidential

Jan 29, 2022

Mr Alla Prudvi Kumar Reddy
H.No 1-15-18, Kakani Vari street
Kavali 524201

ar Alla,

Subject:**Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as **an Academic Intern** at grade **0.2** with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

All terms and conditions in this document, read with any other document specifically referred herein and incorporated hereto by such reference, collectively shall constitute the entire understanding between the Academic Intern and the Company.

Company does not assure you or commit (a) any extension of this internship beyond the period stipulated under this letter and/or offer you employment with Company and/or absorb you as an employee of the Company in future. Unless otherwise specifically agreed in writing by pany, there shall be no employee-employer relationship between you and Company.

1. Working days
Normal working days for Company are Monday through Friday. Company observes Sunday as a compulsory weekly off and Saturday as the other weekly off day. The normal working hours are forty five hours per week.

2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

3.Termination of Internship

The internship can be terminated with one week notice or stipend (if you are eligible for stipend under this letter), in lieu of the notice period on either side.

The Company can terminate your internship without any notice period in case the internship is terminated on grounds of:

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2	Certificate of Graduation/Post Graduation and Mark Sheets
3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

1

Offer Letter Body

Persistent

Reference: Persistent/Academic Intern/1637534/0.2

Internship Offer Letter
Confidential

Jan 29, 2022

Mr Alla Prudvi Kumar Reddy
H.No 1-15-18, Kakani Vari street
Kavali 524201

ar Alla,

Subject:**Your engagement as an Academic Intern with Persistent**

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The duration and start date of the internship will be communicated to you in due course of time separately.

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2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

1

Offer Letter Body

Persistent

Reference: Persistent/Academic Intern/1614897/0.2

Internship Offer Letter
Confidential

Feb 02, 2022

Mr Pusala Hemanth
Mopur vellampalli(Village),Dakkili(Mandal)
Andhra Pradesh
Sri Potti Sriramulu Nellore District 524134

Dear Pusala,

Subject:**Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as **an Academic Intern** at grade **0.2** with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

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4. Dispute Resolution

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Please contact **Rajeshwari Joshi** (Ph. No.**020-66965038**) on the date of joining. We request you to report at 9 am at the address mentioned below for completion of joining formalities.

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3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

PSL/ HR Letter / 2022
05-Aug-2022

Persistent

To Whomsoever It May Concern

This is to certify that **Mr.Karusala Sasank** (Employee Code:49323.1) has worked with our company from 17 Feb 2022 to 15 Jul 2022.

His designation at the time of leaving was Intern.

For Persistent Systems Limited,

Manisha Tapaswi
General Manager - Human Resources

Gmail vanteru hemalatha <vhema575@gmail.com>

Mindtree Digital Practicum | 2022 Batch 8th Semester Internship Offer

1 message

Mindtree Campus <Campus@mindtree.com>
To: "vhema575@gmail.com" <vhema575@gmail.com>

Fri, Feb 25, 2022 at 12:18 AM

24-02-2022

To,
Vanteru Hemalatha,
PARVATHAREDDY BABUL REDDY VISVODAYA INSTITUTE OF TECHNOLOGY AND SCIENCE
Andhra Pradesh

Dear Vanteru Hemalatha,

We are pleased to offer you an **internship** opportunity at **Mindtree Limited**. The terms and conditions of this offer are as follows and your Internship will be subject to and governed by these terms and conditions which shall be binding upon you when you accept this offer by counter-signing this letter.

Internship Duration	:	**14-16 Weeks**
Commencement Date	:	**28th Feb 2022**
Location	:	**Remote Online**
Stipend	:	**Milestone based - Refer 12.**

Additional Terms:

1. You acknowledge that the purpose of this Internship is to provide you with the opportunity to learn generally about information technology work and to gain practical experience and insights of the workplace and industry, and Mindtree does not derive an immediate advantage from the activities performed by you during the Internship Duration.

2. The Stipend stipulated above is payable per month as consideration for the Internship, shall accrue from day to day and shall be paid monthly in arrears, subject to applicable statutory and other deductions, and applicable tax withholdings. Any costs and expenses borne by you in connection with the Internship shall be your sole responsibility.

3. You may be permitted to be absent during the Internship Duration after obtaining prior approval from your Mentor and your stipend may be reduced, at Mindtree's sole discretion and option, by the period of your absence. Prolonged, frequent, or unapproved absences may lead to immediate termination of your Internship upon notice from Mindtree.

4. While with us, you will be required to adhere to policies / practices of Mindtree as applicable to you in your capacity as an intern and as amended from time to time solely at the discretion of Mindtree ("**Policies**"). These policies will be shared with you before your internship commences and during the Internship Duration.

5. **Confidentiality:** As an intern, you will be privy to, have access to or receive Confidential Information (as defined below). You shall (i) use such Confidential Information solely in relation to and to fulfill your Internship; (ii) disclose Confidential Information only to such persons and as permitted in writing by Mindtree; (iii) treat the Confidential Information with all reasonable care; and (iv) return all Confidential Information (and all copies thereof) to Mindtree immediately upon termination or completion of your Internship. Your obligations to maintain secrecy and confidentiality of the Confidential Information shall continue after termination of your Internship with Mindtree.

"***Confidential Information***" *which means any information, data or non-public business, commercial, personal or technical information of Mindtree, its affiliates, parent company, their personnel or that of their clients including but not limited to research and development projects, services, and business operations, which may be disclosed in writing, orally, electronically, by or on behalf of Mindtree. Any documents and information, which reflect, incorporate and/or are generated using any such Confidential Information, will also be deemed as Confidential Information. All Confidential Information shall be deemed as Mindtree's trade secrets.*

6. **Intellectual Property:** Title, interest and ownership in all information, data, outputs, reports, codes, proprietary information or rights, materials, tools presentations, records and intellectual property rights conceived, created or developed by you in connection with or arising from your Internship, and/or making use of the Confidential Information shall vest solely and exclusively with Mindtree immediately upon creation without the need for any further act or payment of any remuneration. It is clarified that Section 19(4) of the Indian Copyright Act, 1957 shall not apply to any assignment of copyrights under this Letter and you hereby agree not to raise and waive all rights to raise, any objection or claim before the Indian Copyright Board with respect to the assignment pursuant to Section 19A of the Indian Copyright Act, 1957. Also, you may conceive newer and advanced methods to improve processes or systems during your internship, this will remain the sole property of Mindtree.

7. You agree to defend, indemnify and hold harmless Mindtree for any loss, liability, claim, costs, fines and or damage suffered by Mindtree and its personnel as a consequence of any breach by you of this Letter, Mindtree's instructions or any Policies.

8. Mindtree, at its sole discretion and option, reserves the right to withdraw, suspend and/or amend the offer of Internship and the terms of this Letter at any time prior to the Commencement Date specified above, and you acknowledge and agree that any such action and/or amendment by Mindtree shall be binding upon you immediately without any consequence on Mindtree.

9. You will be an Intern for the Internship Duration. This Letter and the Internship Duration may be suspended, terminated or reduced (as appropriate) immediately with notice from Mindtree to you.

10. Issuance of Internship Certificate is always subject to the successful completion of the entire Internship Duration and at the sole discretion of Mindtree.

11. Mindtree may receive and collect personal data relating to you, including sensitive personal data or information (as defined in the Information Technology Act 2000 and rules made thereunder) (collectively "**Personal Information**"). Mindtree may process such Personal Information for relevant and limited purposes in connection with managing your Internship and/or the business of Mindtree. You consent to (i) collection, use, processing, storage, export, and transfer of your Personal Information by Mindtree and third parties; and (ii) the transfer and disclosure of your Personal Information held by Mindtree to any third parties within India or outside of India, in accordance with the Mindtree's privacy policy and subject to applicable law.

12.

Internship Milestone	Stipend (INR)
Foundation 1 Valuation & Milestone 2 Valuation	10,000
Milestone 3 Valuation & Milestone 4 Valuation	10,000
Milestone 5 Valuation & Final Comprehensive Milestone 6 Valuation	10,000

The stipend amount for every milestone accomplished in the current month will be credited in the payroll cycle of the consecutive month

This Letter contains the entire understanding between you and Mindtree for your Internship and supersedes all previous discussions and agreements, whether oral or otherwise.

You agree and acknowledge that the Internship is being granted solely for training purposes and that you are not an 'employee' or a 'workman' of Mindtree for the purposes of any employment statute or under any law, and you are not entitled to any wages or any employment benefits (including but not limited to leave and statutory benefits) that are provided solely to employees of Mindtree. You further agree and acknowledge that there is no assurance or guarantee that you will be employed by Mindtree upon completion of the Internship and this Internship is not a guarantee, promise, offer or indication of any future association or relationship with Mindtree.

This Letter and the relationship between us shall be governed by the laws of India and the courts at Bangalore, Karnataka, shall have exclusive jurisdiction over any disputes that may arise therefrom. Mindtree may apply for injunctive or other appropriate relief from any court of competent jurisdiction.

This offer of Internship is valid until 28 Feb 2022 and if not accepted by such date or in case you fail to join us on the Commencement Date, we will assume that you have declined this offer of Internship which shall consequently stand withdrawn immediately.

You agree that your electronic signature below will have the same force and validity as a handwritten signature, and that your signature represents your acceptance of this Letter and your agreement to abide by the terms herein.

We are confident that you will enjoy your experience with us and that the learning you derive will be mutually beneficial.

Looking forward to seeing your expertise in action soon!

Thanking You,

For Mindtree Limited,

Rosalee

Rosalee M Kombial

Vice President – People Function

AGREED AND ACCEPTED:

Signature:

Name:

Date:

March 4, 2022

Dear CHENNAREDDY REDDY,

Sub: Letter of Engagement as Intern

We are pleased to inform you that you have been selected for undergoing Internship in our organization Wipro Limited (Wipro) as Intern under the following terms and conditions:

1. Nature of Engagement

You will be engaged as an **Intern at Wipro**.

2. Duration of training

The duration of **internship** will be 10 to 16 weeks starting from March 10th. During this period, Wipro shall evaluate your performance. Unless Wipro extends the period of internship, in writing, solely at its discretion, your internship shall automatically stand terminated at the expiry of the internship period.

3. Verification Report

Your engagement with Wipro will be subject to receipt of satisfactory report with regard to verification of the particulars furnished by you in your application and information given at the time of Interview. If any declaration or information furnished to Wipro proves to be false or if you have wilfully suppressed any material information, in such case, you will be liable to removal from training without any notice.

4. Obligations and Responsibilities

a. During your internship period, Wipro expects you to undergo training in any department / section in which you are placed with high standard of initiative and efficiency. You shall devote yourself exclusively for undergoing training. You shall not take up any other work for remuneration (part-time or otherwise) or work on advisory capacity or be interested directly or indirectly in any other trade or business (except as share-holder or debenture holder) during the training period without obtaining permission in writing from the appointing authority at Wipro. You will be governed by the service rules / standing orders, policies and regulations as may be promulgated by Wipro from time to time in relation to conduct, discipline and other matters. You will not seek membership of any local or public bodies without first attaining specific permission from the appointing authority at Wipro. You are expected to comply with the policies of Wipro including the Code of Business Conduct and other policies of Wipro as they form an integral part of the terms of your training with Wipro.

   Consequently, you are required to understand the scope and intent behind these policies and to comply with the same. These Policies are updated / modified on a periodic basis and new Policies may be introduced and notified to employees/trainees from time to time and you will be required to comply with the same. Any matter or situation or incident that may arise that could potentially result, or has resulted, in any violation of the Policies or the terms of your employment, shall immediately be brought to the notice of Wipro and appropriate disciplinary action will be initiated.

b. During the training period, if you conceive any new or advanced method of improving processes / formulae / systems in relation to the Business or Trade of Wipro, such developments will be fully communicated to Wipro and will be the sole property of Wipro. In consideration of the opportunities, training and access to new techniques and know-how that will be made available to you, you will be required to comply with the Confidentiality Policy of Wipro. Therefore, please maintain all Confidential Information as defined from time to time in the Confidentiality Policy of Wipro, as secret and confidential and do not use or disclose any such Confidential Information except as may be required under obligation of law or as may be required by Wipro and in the course of your training. This covenant shall endure during your training and beyond the cessation of your training with Wipro.

c. During the training period and thereafter, you will not pass onto anyone in writing or by word of mouth or otherwise, particulars or details of work, processes, technical know-how, research carried out, security arrangements, administrative and organization matters of confidential or secret nature, which you may come across during your training period or become known to you by virtue of your undergoing training in Wipro or otherwise.

d. In connection with your internship and during the term of your internship, upon conception or creation, you shall disclose and assign to Wipro as its exclusive property, all inventions, ideas, concepts, discoveries, techniques, and improvements (including without limitation legal documents, training materials, computer software and associated materials) developed or conceived by you solely or jointly with others (whether or not during business hours), and shall comply with the Policies of Wipro in relation to Intellectual Property.

5. Posting

During your training period, you are liable to be transferred or assigned to training in any division / department / establishment or location at which Wipro or its associate companies have their offices or operation and whether at present existing or which may be set up in future at any time and at any place in India, without any increase in stipend. On such posting, you will be governed by the policies, rules and regulations as applicable in that Unit / Branch / Establishment.

6. Travel

You will be required to undertake travel as required by Wipro and you will be paid travel expenses as per Wipro rules.

7. Termination

Notwithstanding any of the clauses of this letter of engagement, Wipro reserves the right in its sole discretion of terminating this agreement during the training period without assigning any reason by giving one week's (7 days) notice or payment of one week's stipend, in lieu of notice.

8. Training Hours and Holidays

As an intern you will be called upon to undergo training during the hours and days as may be fixed by Wipro. Normally all Sundays will be weekly holidays together with all National and Festival Holidays observed by the establishment.

9. After completion / termination of internship

On completion / termination of internship, you will immediately surrender to Wipro all specifications, documents, literature, drawings, records etc. belonging to Wipro or relating to its Businesses and shall not take or retain any copies of the said items.

10. Date of commencement of training

In case the above terms and conditions are acceptable to you, you are required to return the duplicate copy of this letter of engagement within one week, duly signed by you, in token of your acceptance of the offer and report for training on or before the date of commencement of training. While reporting for training, please bring 3 copies of your latest passport size photographs and two copies each of your certificates and testimonials along with the originals. The original certificates will be returned to you after verification.

Yours sincerely,
For Wipro Limited,

Aparna Shailen
General Manager - Human Resources

Endorsement:

1. I accept the terms and conditions stipulated in the above letter of engagement.

2. I shall report for internship on

ANNEXURE I

CONFIRMATION ON SHARING PERSONAL INFORMATION (AS REQUIRED UNDER INFORMATION TECHNOLOGY ACT, 2000)

I CHENNAREDDY REDDY, confirm that I am voluntarily sharing my Personal Information with Wipro Limited ('Wipro') for the following purposes:

a. validating my curriculum vitae and retaining records on the same for any future reference/verification;

b. processing my application for internship including background verification checks;

c. Internship related actions including record keeping, processing training stipend and any action required in the context of my training with Wipro.

In this context, I also agree to the retention of such Personal Information by Wipro for any future reference/verification and authorize Wipro to transfer the same to a third party.

I understand that 'Personal Information' means any information, relating to me that is available with Wipro and is capable of identifying me.

ANNEXURE II

CONFIDENTIALITY & NON-DISCLOSURE AGREEMENT

This non-disclosure agreement ("**Agreement**") is made on this the [ ] day of [ ] between

Wipro Limited, a public limited Company incorporated under the Indian Companies Act, 1913, and existing under the Indian Companies Act, 1956, having its registered office at Dodda Kannelli, Sarjapur Road, Bengaluru 560-035.

And

_____[Name of the Intern], S/o / D/o

_____.

Residing at_____

_____

(Hereinafter referred to as "**Intern**" which expression shall mean and include his/her representatives in interest, assurers and guarantors).

WHEREAS:

The Intern has expressed his/her desire to be trained with Wipro for a period of _____ ("**Internship Period**");

Wipro has accepted the Intern's application subject to the Intern adhering to and complying with certain covenants governing his or her movement within Wipro premises, conduct, and other tasks whatsoever which they may be allotted from time;

During the term of the internship, the Intern may have access to certain information which may be proprietary and/or of confidential nature ("**Confidential Information**", as more particularly described below).

NOW THEREFORE in consideration of the Agreement herein by the parties hereto and such additional promises and understandings as are hereinafter set forth, the parties agree as follows:

1. For purposes of this Agreement, "**Confidential Information** "means, with respect to Wipro, any and all information in written, representational, electronic, verbal or other form that is disclosed to Intern by Wipro or which Intern becomes aware of in the course of the internship, including without limitation, information relating directly or indirectly to the present or potential business, operation or financial condition, pricing, legal cases pertaining Wipro, marketing plans or strategy, volumes, services rendered, customers' and suppliers' names or lists, any customer information, financial or technical or service matters or data of or relating to Wipro and any information identified as being proprietary and/or confidential and any information which might reasonably be presumed to be proprietary or confidential in nature, excluding any such information which (i) is known to the public (through no act or omission of Intern in violation of this Agreement); (ii) was known to Intern prior to its disclosure under this Agreement; or (iii) is required to be disclosed by governmental or judicial order, in which case Intern shall give Wipro prompt written notice, and use reasonable efforts to ensure that such disclosure is

accorded confidential treatment and also to enable Wipro to seek a protective order or other appropriate remedy.

2. Nothing contained hereunder shall be construed as creating, conveying, transferring, granting or conferring by Wipro on Intern any rights, license or authority in or to the Confidential Information.

3. Intern agrees and undertakes that he/she shall not disclose or make available to any person (including the Institute) reproduce or transmit in any manner, or use (directly or indirectly) for his/her own benefit or the benefit of others, any Confidential Information, including without limitation, the use of the Confidential Information in any thesis or report required to be submitted by Intern under any course. Intern undertakes that he/she will not, without prior written consent of Wipro, use any Confidential Information in any of her future projects or presentations for any person, including the institute, nor shall he/she use any of the Confidential Information in his/her resumes or any application for prospective employment.

4. Intern shall use and/or protect the Confidential Information received by him/her with utmost degree of care and diligence.

5. Intern agrees that upon (i) termination/expiry of Internship Period, or (ii) at any time during its currency, or (iii) on Intern ceasing to be an Intern of Wipro, Intern shall promptly deliver to Wipro the Confidential Information and copies thereof in his/her possession or under his/her direct or indirect control, and shall destroy all memoranda, notes and other writings prepared by him/her or his/her subordinates based on the Confidential Information.

6. Intern acknowledges that the Confidential Information coming to his/her knowledge may relate to and/or have implications regarding the future strategies, plans, business activities, methods, processes and or information of Wipro or its affiliated companies which could afford third parties certain competitive and strategic advantage. Intern shall ensure that the use of such Confidential Information by the Intern shall not jeopardize or adversely affect in any manner such future strategies, plans, business activities, methods, processes, information, and/or competitive and strategic advantage of Wipro.

7. Intern acknowledges the quantum of damages and/or losses that Wipro may suffer as a result of the breach of this Agreement by the Intern and therefore, agrees to indemnify and keep indemnified Wipro against all loss or damage, which Wipro may suffer as a result of any such breach.

8. Intern hereby acknowledges and agrees that in the event of a breach or threatened breach by Intern of the provisions of this Agreement, Wipro shall without prejudice to any of its rights under this Agreement or in law have the right to claim damages and shall also be entitled to injunctive relief against such breach or threatened breach by Intern.

9. No failure or delay by Wipro in exercising or enforcing any right, remedy or power hereunder shall operate as a waiver thereof, nor shall any single or partial exercise or enforcement of any right, remedy or power preclude any further exercise or enforcement thereof or the exercise of enforcement of any other right, remedy or power.

10. This Agreement will be governed exclusively by the laws of India and, jurisdiction shall be vested exclusively in the courts at Bengaluru. This Agreement shall not be amended, assigned or transferred by either party without obtaining the written consent of Wipro.

11. The obligations of confidentiality shall survive the expiry or termination of the internship. Nothing in this Agreement is intended to confer any rights/remedies under or by reason of this Agreement on any third party.

12. If any term or provision of this Agreement is determined to be illegal, unenforceable, or invalid in whole or in part for any reason, such illegal, unenforceable, or invalid provisions or part(s) thereof shall be stricken from this Agreement and such provision shall not affect the legality, enforceability, or validity of the remainder of this Agreement.

IN WITNESS WHEREOF the parties hereto have duly executed this Agreement as of the date and year written above.

Yours sincerely,
For Wipro Limited,

Aparna Shailen
General Manager - Human Resources

☑ Accept ☐ Decline

Intern Name: CHENNAREDDY REDDY

☑ **Signature** CHENNAREDDY REDDY 4/3/2022 2:55 PM
(checking the checkbox above is equivalent to a handwritten signature)

Registered Office:

Wipro Limited
Doddakannelli
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PSL/HRLetter/2022
29-Aug-2022

Persistent

To Whomsoever It May Concern

This is to certify that **Ms.Ramala Sahithi** (Employee Code:49833.1) has worked with our company from 17 Feb 2022 to 15 Jul 2022.

Her designation at the time of leaving was Intern.

For Persistent Systems Limited.

Manisha Tapaswi
General Manager - Human Resources

Persistent

Reference: Persistent/Academic Intern/1615695/0.2

Internship Offer Letter
Confidential

Feb 02, 2022

Ms DevaHarshini Gadamsetty
5-17-25, bhaskarunivaristreet, nearfivelampscenter,kavali,Nellore dt
Kavali 524201

Dear DevaHarshini,

Subject:**Your engagement as an Academic Intern with Persistent**

With reference to your application for industrial training with us, and the subsequent selection process, we are pleased to inform you that you have been selected as an **Academic Intern** at grade 0.2 with Persistent Systems (Company). This offer is made to you as part of your Academic Curriculum.

The duration and start date of the internship will be communicated to you in due course of time separately.

During the internship period you will be paid a consolidated monthly stipend of Rs. 10,000 per month. You will also be eligible for benefits such as free lunch, snacks, tea and coffee during your internship period.

All terms and conditions in this document, read with any other document specifically referred herein and incorporated hereto by such reference, collectively shall constitute the entire understanding between the Academic Intern and the Company.

Company does not assure you or commit (a) any extension of this internship beyond the period stipulated under this letter and/or offer you employment with Company and/or absorb you as an employee of the Company in future. Unless otherwise specifically agreed in writing by Company, there shall be no employee-employer relationship between you and Company.

1. Working days
Normal working days for Company are Monday through Friday. Company observes Sunday as a compulsory weekly off and Saturday as the other weekly off day. The normal working hours are forty five hours per week.

2. Holidays and Leaves
You will not be eligible for any leave or compensatory off during internship period.

3.Termination of Internship
The internship can be terminated with one week notice or stipend (if you are eligible for stipend under this letter), in lieu of the notice period on either side.

The Company can terminate your internship without any notice period in case the internship is terminated on grounds of:
i. Breach of confidentiality or IP related obligations
ii. Violation of law
iii. Gross Misconduct
iv. Material breach of Company policy.

In such event, the Company will not be liable to pay stipend (if payment is otherwise stipulated in this letter) in lieu of notice period.

In case the last day of your internship falls on a non-working day, your last day of internship shall be the immediate previous working day.

The internship period can be terminated by whatsoever reasons by either party by giving one week notice period.

4. Dispute Resolution
In case of any dispute or disagreement in relation to the terms of this offer or matters connected thereto, you agree to negotiate in good faith to resolve such dispute or disagreement. In case you and Company fail to settle the dispute/ disagreement amicably, the same may be exclusively referred to arbitration in accordance with the provisions of Arbitration and Conciliation Act, 1996 at Pune. Each party shall bear its own costs for arbitration.

Please contact **Rajeshwari Joshi** (Ph. No.**020-66965038**) on the date of joining. We request you to report at 9 am at the address mentioned below for completion of joining formalities.

Pune
Rigveda-Yajurveda-Samaveda-Atharvaveda Plot No. 39, Phase I, Rajiv Gandhi Information Technology Park,Hinjawadi,Pune, Maharashtra, India 411057.

5. Documents required at the time of joining
At the time of joining, the following original certificates/documents along with one photocopy should be furnished.Original certificates/documents will be returned to you after verification.

Sr. No	Description
1	Certificates of educational qualification - SSC (10th Equivalent), School leaving, HSC (12th equivalent),
2	Certificate of Graduation/Post Graduation and Mark Sheets
3	2 recent passport size color photographs
4	Photo-attested bonafide certificate from college Principal

We welcome you to the Persistent family and look forward to a mutually fulfilling association.

Yours sincerely,
For Persistent Systems Ltd

Kalpana Kudlingar
Head - Campus Talent Acquisition

Acceptance of the offer

I have read and understood all the terms and conditions contained in this letter and agree to abide by the same. I am signing this letter as a token of me having accepted the offer and the terms and conditions set out in this letter.

Also, I hereby declare that nothing apart from the above mentioned clauses have been committed to me during the selection process.

I will join the Company on the date communicated to me separately.

Date:

Signature:
Name:

Design and Product Development of a Dual Channel Line Impedance Stabilization Network for Electromagnetic Interference Compatibility

Publisher: IEEE

A. Bhakthavachala ; K. Anuradha ; S. Tarakalyani All Authors

Abstract

Abstract:
the production of intelligent technology apparatus is drastically increasing in consumer-side applications and at the same time, the high-frequency noises are being injected into the sources of various grids. So to maintain the quality of apparatus life there have been some differential and conducted emission tests that are needed to be carried out both in industrial and domestic applications where the apparatus are connected to the power supply. In this

Computer Networks and Inventive Communication Technologies pp 1113–1125

Design and Analysis of Rectangular Microstrip Patch Antenna for 2.4 GHz Wireless Communication Applications Using CST Microwave Studio

V. Prakasam, P. Sandeep & K. R. Anudeep LaxmiKanth

Conference paper | First Online: 03 June 2021

Part of the Lecture Notes on Data Engineering and Communications Technologies book series (LNDECT,volume 58)

Abstract

In this paper, the operating frequency or resonance frequency of 2.4 GHz is selected, which is best for industrial, scientific and medical (ISM) band applications. CST MWS is used as the software environment to design and simulate the performance of the antennas. The dimensions of a rectangular microstrip patch antenna have 38 mm × 29 mm × 0.13 mm. This antenna is designed using lossy FR-4 substrate material used as a dielectric with reduced size of 76 mm × 58 mm. Its dielectric constant is 4.4 and 1.6 mm thickness. This paper

presents CST Microwave Studio. Here, VSWR plot, 2D Radiation pattern plot, S-parameter magnitude, bandwidth plot, directivity polar plot, E-Field, H-Field, Surface current and gain of the antenna are estimated using CST microwave studio software.

Keywords

Microstrip patch antenna **CST** **ISM**

VSWR **Edge feed technique**

Radiation pattern **S-parameter**

Recent Study on Power Efficient Arithmetic Circuits for Low Power Applications

G. Navabharat Reddy ; P. A. Harsha Vardhini ; V. Prakasam ; P. Sandeep

New Approaches in Engineering Research Vol. 9, 3 August 2021, Page 78-98
https://doi.org/10.9734/bpi/naer/v9/11414D
Published: 2021-08-03

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Abstract

Low power consumption is required for integrated circuit design in nanometerscale CMOS technology.

Recent research shows that, when compared to accurate designs, implementing approximate designs results in lower power dissipation. DSP blocks have been used as the core blocks in the majority of multimedia applications. The majority of video and image processing algorithms are implemented by these DSP blocks, with the end result being an image or video for human viewing. Because the human sense of observation is limited, the output of the DSP blocks allows for numerical approximation

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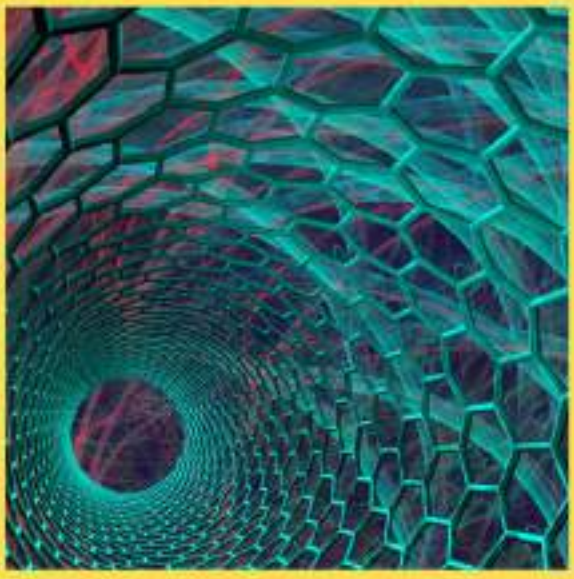
Current Research of Nanotechnology in Science and Engineering Volume I



Editor:
Dr. Bassa Satyannarayana

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First Edition: 2022

CURRENT RESEARCH OF NANOTECHNOLOGY IN SCIENCE AND ENGINEERING

Volume I

It's a Present & Future Technology

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Editor

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PREFACE

Nanotechnology is one of the most promising technologies of the twenty-first century. Nanotechnology is described as the design, development, and implementation of materials and technologies on the nanoscale with the smallest functional components (1 to 100 nm). Nanotechnology covers a wide range of issues, from standard device physics and chemistry extensions to entirely new techniques based on molecular self-assembly, from developing new Nano size materials to investigating whether we can directly alter matter at the atomic scale level.

Nanotechnology can be used in a variety of fields, including medical, agriculture, and environmental protection. Many diseases for which there are presently no treatments may be treated in the future as a result of nanotechnology. The use of nanotechnology in medical therapy needs a careful examination of its risks and potential side effects. Even scientists who oppose the use of nanotechnology agree that advancement in the field should continue since it offers enormous benefits, but more testing is needed to ensure its safety in people. Nano medicine may play a key role in the treatment of human and plant disorders, as well as the enhancement of normal human and plant physiology and systems, in the future.

Nanoscience and nanotechnology are the study and application of extremely small objects, with applications in chemistry, biology, physics, materials science, and engineering, among other fields. Nanotechnology is being used in a range of energy-related applications, including increasing the efficiency and cost-effectiveness of solar panels, producing new types of batteries, boosting fuel production efficiency through better catalysis, and building better lighting systems. Nano science and nanotechnology applications in engineering connect academic research in Nano science and nanotechnology to industry and everyday life. As a result, a diverse range of nanomaterials, nano devices, and nano systems have been developed and deployed for human benefit in a number of technical applications.

Nanoscience and Nanotechnology in Engineering is based on the authors' numerous lectures and courses given all over the world. Nanotechnology has also helped to design more efficient and long-lasting materials, such as self-cleaning and self-repairing concrete and windows. Coatings based on nanotechnology can help with fire protection, corrosion resistance, insulation, and a range of other applications. All scientists, academicians, researchers, and students working in the fields of chemistry, biology, physics, materials science, and engineering, among other fields, will find this book quite valuable.

This book with valuable book chapters from eminent scientists, academicians, and researchers will surely be a part of utmost information for the coming new research taken by the researchers in the field of chemistry, biology, physics, materials science, and engineering, among other subjects.

ABOUT THE BOOK

As scientists endeavour to comprehend the mechanisms of natural and biomolecular computing, Nano scale science and computing is becoming a key research subject. The architecture and design of molecular self-assembly, nanostructures, and molecular devices, as well as understanding and harnessing the computational processes of biomolecules in nature, are all topics in this discipline.

This book provides a unique and authoritative view of contemporary Nano scale science, engineering, and computing research. The book is appropriate for academic and industrial scientists and engineers working in Nano scale science, particularly those interested in molecular level computing.

Nano science and nanotechnology are the study and application of extremely small objects, and they can be applied in chemistry, biology, physics, materials science, and engineering, among other subjects. Nanotechnology is being employed in a variety of energy-related applications, including improving the efficiency and cost-effectiveness of solar panels, developing new types of batteries, improving the efficiency of fuel production through better catalysis, and developing better lighting systems. Engineering's application of Nano science and nanotechnology connects academic research in Nano science and nanotechnology to industry and everyday life. As a result, a wide range of nanomaterial's, Nano devices, and Nano systems for a variety of technical applications have been produced and deployed for human benefit. Nano science and Nanotechnology in Engineering is based on the many lectures and courses presented around the world by its authors. Nanotechnology has also aided in the development of more efficient and long-lasting materials, such as self-cleaning and self-repairing concrete and windows. Nanotechnology-based coatings assist in increasing fire resistance, corrosion resistance, insulation, and a variety of other uses. This book is very useful to all scientists, academicians, researchers and students in the field of chemistry, biology, physics, materials science, and engineering, among other subjects.

This book with valuable book chapters from eminent scientists, academicians, and researchers will surely be a part of utmost information for the coming new research taken by the researchers in the field of chemistry, biology, physics, materials science, and engineering, among other subjects.

Dr. Bassa Satyannarayana
Editor

CONTENT

Progress In Electromagnetics Research C, Vol. 115, 277–289, 2021

Artificial Neural Network Based SIW Bandpass Filter Design Using Complementary Split Ring Resonators

Ranjit Kumar Rayala* **and Raghavan Singaravelu**

Abstract—A novel Artificial Neural Network (ANN) based two Substrate integrated waveguide (SIW) bandpass filters comprising Complementary Split Ring Resonators (CSRRs) are proposed in this paper. These CSRRs are modelled on the upper layer of the SIW cavity. A feed forward multilayer perceptron (FF-MLP) neural network is used to optimize the physical dimensions of the proposed filters. To validate the analytical results, physical prototypes of the proposed filters are fabricated, and a measurement is carried out with a Combinational Network Analyzer (Anritsu-MS2037C), and the obtained experimental results agree well with the estimated results using full wave analysis. Within the passband from 8.22 to 8.95 GHz, S_{12} of the first filter shows better than -0.5 dB insertion loss (IL) and a fractional bandwidth of 8.5%, and within the passband from 8.21 to 8.73 GHz, the second filter shows IL about -0.8 dB and a fractional bandwidth of 6.1%.

1. INTRODUCTION

Substrate Integrated Waveguide (SIW) filters have recently attracted a lot of attention because of their high efficiency, easy fabrication process with simple printed circuit board (PCB) technology, small size, low insertion loss, high selectivity, and ease of integration with microwave and millimetre wave circuits [1, 2]. In modern communication systems, one of the important requirements is miniaturization. SIW bandpass filter has been designed and investigated using slow wave method [3, 4]. SIW structures are typically composed of conducting vias which are placed in a dielectric substrate that connects two parallel metal plates, enabling the use of traditional rectangular waveguide components in planar form. The conventional PCB technique can be used in SIW based passive, active devices, microwave components, and antennas. The latest developments in SIW technology in terms of its modelling, design, and technological implementation of SIW structures and components have been reported [5–8]. To acquire compact size and modular geometry, a new type of quasi-elliptic pass-band filters based on mushroom-shaped metallic resonators in SIW technology has been proposed [9]. SIW bandpass filter with a cross-shaped cavity that realizes six symmetrically simulated modes out of first eight higher order resonant modes has been proposed [10]. An SIW band-pass filter having wide and sharp stop band, which differs from filters with a direct coupling between input and output has been proposed [11]. An SIW bandpass filter, modelled on a double layer dielectric substrate consisting of metallic via holes in order to realize the classical H-plane filter has been proposed [12]. Two cascaded mushroom resonators have been modelled on the SIW cavity that works as a dual band bandpass filter has been presented [13]. On the waveguide top metal layer, a number of cross-slot patterns have been modelled to act as dual mode SIW filters [14].

The performance of SIW filters can be improved by using some special types of electromagnetic topologies like split ring resonator (SRR) and complementary split ring resonator (CSRR) and have been

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adapted into SIW technology [15]. A novel diamond-shaped CSRR has been proposed and investigated based on an SIW bandpass filter [16]. An extended doublet bandpass filter that uses an SIW cavity with CSRRs on the top layer has been proposed, and a single layer bandpass filter with two transmission zeros (TZ) was analyzed [17]. An SIW filter with square CSRRs has been proposed, and the characteristics of passband have been observed by varying the directions of the CSRRs [18]. CSRR has been modelled on the top surface of the SIW that provides a passband below the initial cutoff frequency of the waveguide TE_{10} mode [19]. By loading CSRRs onto the SIW cavity, the SIW bandpass filters have been achieved in compact size and high selectivity [20]. A double sided CSRR half mode SIW filter that provides lower resonant frequency than the conventional model because of the coupling effect between CSRRs of the upper and lower plates has been proposed [21]. Based on evanescent-mode propagation, a compact SIW bandpass filter using broad side coupled CSRR [22] and fractal open complementary split-ring resonators (FOCSRRs) unit-cell has been presented [23]. Complementary open-ring resonators (CORRs) loaded half mode substrate integrated waveguide (HMSIW), with many transmission zeros and wide stopband, have been proposed [24]. Novel dual mode SIW filters that can provide multiple transmission zeros have been proposed [25].

One of the issues with designing SIW components and RF circuits in the above literature is that the simulation actually needs a lot of calculations, so optimization of the parameters takes a very long time. ANN has been chosen as an alternative method to design microwave circuits and devices, hence ANNs have been used to design circular and rectangular resonators modelled in SIW technology [26, 27]. A back-propagation neural network-based approach for modelling the SIW power dividers has been proposed [28]. In order to model and optimize the microwave components and devices, an efficient hybrid sampling method has been proposed to get optimum design parameters by using the ANN model [29].

The main contribution of the proposed research work is a feed forward multilayer perceptron (FF-MLP) neural network that has been used to optimize the proposed filter parameters. In this work, two networks with $2 \times 12 \times 1$ and $1 \times 8 \times 1$ have been used. The trainlm function in MATLAB has been used to efficiently train the FF-MLP neural networks. The S_{11} parameter has been calculated to evaluate the proposed networks, and the results obtained are in good agreement with the simulated results. Instead of a single CSRR, two CSRRs have been employed to enhance the proposed band pass filter's roll-off rate.

This paper is organized as follows. Section 2 explains how the basic topology of the proposed SIW filter is designed. Section 3 explains how the filter parameters are optimized using neural networks. Section 4 shows how the filter was simulated and the simulation results. Section 5 provides the fabrication process, measurement setup, and the measured results plotted against the simulated ones.

2. DESIGN OF CROSS SHAPED SIW CAVITY WITH CSRR

The proposed cross shaped SIW cavity topology is depicted in Figure 1. The basic SIW topology consists of three layers. The perfect electric conductor (PEC) is used as bottom layer and top layer, and the middle layer is dielectric material. The dielectric material used is Roggers RO4003C with dielectric constant $\varepsilon_r = 3.55$ and height of the substrate $h = 0.81\,\text{mm}$. The optimized design dimensions of this SIW cavity are as follows. The length of the SIW cavity is $L = 40.8\,\text{mm}$; the length of the dielectric substrate used is $L_{sub} = 60\,\text{mm}$; the feeding slot length $L_{slot} = 5.4\,\text{mm}$; the feeding slot width $W_{gap} = 1.4\,\text{mm}$; the width of the microstrip line is $W_{mst} = 2\,\text{mm}$; the diameter of the metallic post or via-hole is $d = 1.2\,\text{mm}$. These metallic posts are placed with two different allowable separation distances or pitches (via-to-via distance) of the vias $p = 1.7\,\text{mm}$ and $p_1 = 2\,\text{mm}$. The geometries of this cross shaped SIW cavity in horizontal and vertical directions are the same.

2.1. Design of CSRR

The square shape CSRR is used in the filter design process, and the physical appearance of this CSRR is as depicted in Figure 2. The CSRR acts as an electric dipole, and this CSRR structure is etched on the upper PEC of the SIW cavity. The exited mode of the CSRR is the same as the dominant mode TE_{10} of the SIW cavity.

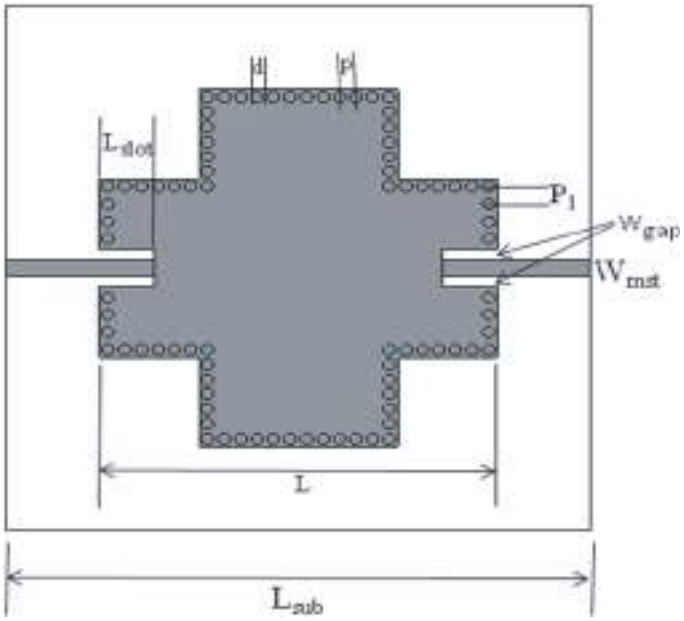


Figure 1. Cross shaped SIW cavity.

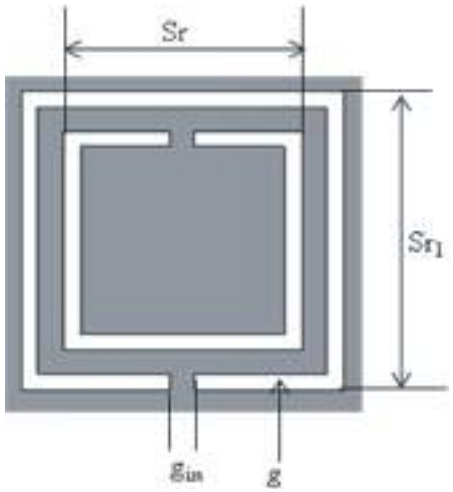


Figure 2. Structure of CSRR.

The CSRR structure resembles an LC resonant circuit. The resonance frequency of the CSRR is computed by the self inductance L and capacitance per unit length C'. The resonant frequency of square shaped CSRR is given by [16]

$$f_r = \frac{1}{2\pi\sqrt{L_0 C_0}} \tag{1}$$

where L_0 and C_0 represent the equivalent inductance and equivalent capacitance of the CSRR structure. The equivalent capacitance C_0 can be derived by using the following expression,

$$C_0 = (C_s + C_g)/2 \tag{2}$$

where C_s and C_g are series and gap capacitances of CSRR, and these two capacitances can be found by using some of the SIW filter parameters like width (w), metal thickness (mt), and free space permittivity (ε_0). In this paper, by using these square shaped CSRRs two SIW bandpass filters are designed.

2.2. SIW Bandpass Filter with Single CSRR

Initially an SIW bandpass filter with single CSRR is designed and fabricated. This design process is done by using SIW crosses shaped topology with the optimized values which have already been mentioned earlier, and then CSRR is loaded into it. The CSRR is etched on the top layer of the structure which is a conducting material (PEC), with the optimized geometrical parameters as follows, $S_r = 2.8\,\text{mm}$, $S_{r1} = 3.8\,\text{mm}$, $g = 0.4\,\text{mm}$, $g_{in} = 0.4\,\text{mm}$, and this total topology is as shown in Figure 3 which is designed and simulated using CST microwave studio. The fabricated prototype model is shown in Figure 9(a).

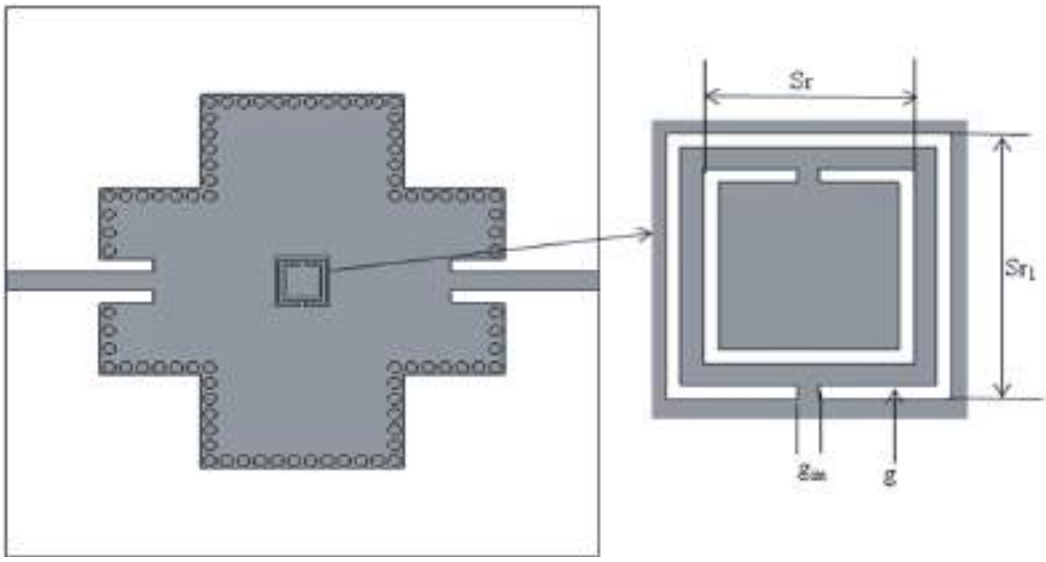


Figure 3. SIW bandpass filter with single CSRR.

2.3. SIW Bandpass Filter with two CSRRs

Another SIW bandpass filter is designed with two CSRR rings facing each other with a separation distance $t = 0.6\,\text{mm}$, and it was fabricated. The optimized values are: $d = 1.2\,\text{mm}$, $L_{sub} = 60\,\text{mm}$, $L = 40.8\,\text{mm}$, $L_{slot} = 5.6\,\text{mm}$, $p = 1.7\,\text{mm}$, $p_1 = 2\,\text{mm}$, $W_{mst} = 1.6\,\text{mm}$, $W_{gap} = 1.4\,\text{mm}$.

Now in this topology two CSRRs are etched on the upper conducting layer (PEC), with the optimized geometrical parameters as follows, $S_r = 2.6\,\text{mm}$, $S_{r1} = 3.4\,\text{mm}$, $g = 0.4\,\text{mm}$, $g_{in} = 0.4\,\text{mm}$, as shown in Figure 4 and designed and simulated using CST microwave studio, and the fabricated prototype model is shown in Figure 9(b).

3. ANN OPTIMIZATION

3.1. Typical Structure of the Artificial Neural Networks (ANN)

The basic structure of ANN shown in Figure 5 consists of three sections. The first section is the input layer; the second section is hidden layer which has one or more sub-layers; and the third section is the output layer. In each stage, there are some processing units which are known as neurons, and all these neurons are interconnected to each other. Each neuron receives some information from one or more other neurons and is processed further. The neural network produces an output which is a weighted sum of all the information from input layer and hidden layer. There are several types of neural networks, which are categorized based on the neuron types and the interconnections between them.

The input to the neurons in the input layer is externally (out of the neural network) applied. The output of the input layer neurons acts as input to the hidden layer neurons. The information is processed

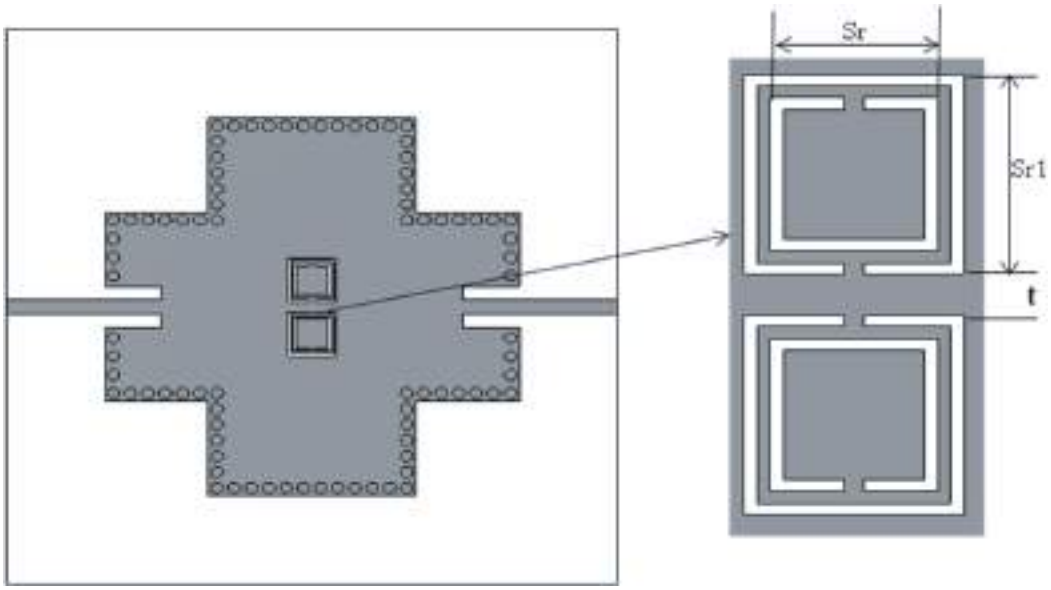


Figure 4. SIW bandpass filter with two CSRRs.

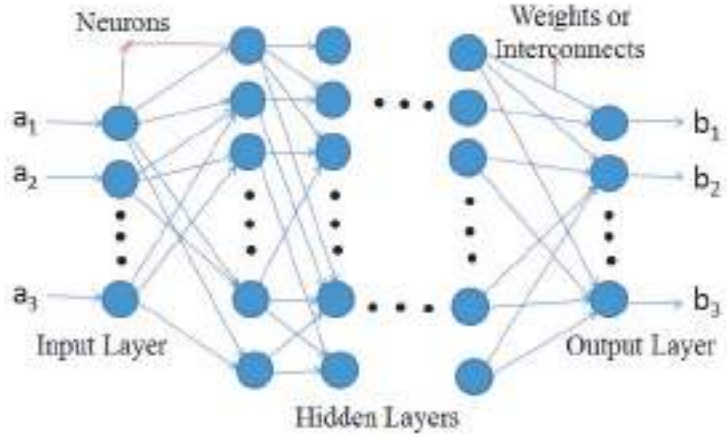


Figure 5. Topology of MLP-ANN.

among all these hidden layer neurons, and finally the output of the hidden layer acts as input to the output layer.

3.2. Filter Parameters Optimization Using ANN

The physical parameters of the proposed filter are optimised by using ANN in MATLAB. Basically there are many types of neural networks. Among them, FF-MLP neural network is used for the optimization of proposed filter parameters.

3.2.1. Neural Network Training

The S_{11} output data collected from the parametric analysis in CST are used as training data, shown in Table 1 and Table 2. Two neural networks are designed to optimize the filter parameters. The first network contains one input layer with two neurons, one hidden layer with 12 neurons, and one output layer with one neuron. In order to train the first network, the data shown in Table 1 are used. The filter

Table 1. Training data for first network.

S. No.	S_r (mm)	S_{r1} (mm)	S_{11} (dB) (CST)
1	2.05	3.05	−8.542
2	2.15	3.15	−10.853
3	2.25	3.25	−11.101
4	2.35	3.35	−11.780
5	2.45	3.45	−12.676
6	2.55	3.55	−13.967
7	2.65	3.65	−16.712
8	2.75	3.75	−20.083
9	2.85	3.85	−23.397
10	2.95	3.95	−18.860
11	3.05	4.05	−18.643

Table 2. Training data for second network.

S. No.	W_{gap} (mm)	S_{11} (dB) (CST)
1	0.75	−11.137
2	0.85	−13.165
3	0.95	−14.766
4	1.05	−16.181
5	1.15	−17.911
6	1.25	−19.915
7	1.35	−22.001
8	1.45	−23.268
9	1.55	−22.185

parameters S_r and S_{r1} are applied to the input layer, and S_{11} is the target value. The second network also consists of one input layer with single neuron, one hidden layer with 8 neurons, and the output layer with one neuron, and it is trained with the data shown in Table 2. The second network is used to optimize the filter parameter W_{gap}. These two neural networks are trained using Levenberg Marquart (LM) algorithm, for which the 'trainlm' function is used, and log-sigmoid is used as transformation function. Adaption learning function (LEARNGDM) is used with a learning rate of 0.01.

The training of this neural network is carried out with a learning method known as supervised learning error back propagation method. In this method, the mean square error is back propagated, and the weights are updated accordingly in order to get minimum error. After training the network with the sample data, the weights of this network remain constant, and the neural network is enough trained. Now the neural network is ready to examine with the testing data.

3.2.2. Neural Network Testing

After enough training, the neural network is ready for testing with the data shown in Table 3 and Table 4, and the final results are also included in the same table. The testing dada and the S_{11} obtained in CST MWS agree well with each other with minimum mean square error.

Table 3. Testing data for first network.

S. No.	S_r (mm)	S_{r1} (mm)	S_{11} (dB) (CST)	S_{11} (dB) (ANN)
1	2.0	3.0	−6.441	-6.5070
2	2.1	3.1	−10.646	−10.5359
3	2.2	3.2	−11.057	−10.8425
4	2.3	3.3	−11.435	−11.2598
5	2.4	3.4	−12.89	−12.9872
6	2.5	3.5	−13.226	−13.3160
7	2.6	3.6	−14.618	−14.7271
8	2.7	3.7	−18.247	−18.3683
9	2.8	3.8	−24.095	−23.9871
10	2.9	3.9	−23.851	−23.8316
11	3.0	4.0	−23.359	−22.7611
12	3.1	4.1	−21.844	−21.9474

Table 4. Testing data for second network.

S. No.	W_{gap} (mm)	S_{11} (dB) (CST)	S_{11} (dB) (ANN)
1	0.8	−12.515	−12.6186
2	0.9	−13.997	−13.7384
3	1.0	−15.505	−15.5065
4	1.1	−17.054	−17.0542
5	1.2	−18.975	−18.4913
6	1.3	−20.912	−20.9320
7	1.4	−23.782	−23.7203
8	1.5	−23.125	−23.5102
9	1.6	−22.344	−22.3218

4. RESULTS AND DISCUSSION

The simulated results are as shown in Figure 6. Figure 6(a) shows the transmission characteristics of the SIW cavity filter with single CSRR slot, which was designed and simulated using CST microwave studio. From the graph it is clear that there are two closely spaced resonances observed at 8.4 GHz and 8.6 GHz, with the passband centre frequency of 8.5 GHz. Significantly one of the resonant frequencies is caused by the CSRR, and the other resonant frequency is because of the SIW cavity. The proposed filter offers a good reflection which is better than −10 dB, and the reflection bandwidth is 485 MHz, from 8.29 to 8.77 GHz. The transmission bandwidth at −1 dB is 480 MHz, and it is between 8.3 GHz and 8.78 GHz. At −3 dB, the transmission bandwidth is 730 MHz, and it is from 8.22 GHz to 8.95 GHz. Within the frequency range from 8.38 to 8.64 GHz, the return loss is smaller than −24 dB.

Figure 6(b) presents the transmission characteristics of proposed SIW band pass filter with two CSRR slots. At −1 dB, the bandwidth obtained is 410 MHz, ranging from 8.27 to 8.68 GHz, and the bandwidth considered at −3 dB is 530 MHz, which is from 8.21 to 8.73 GHz, with the centre frequency of 8.5 GHz. This filter also shows two resonant frequencies, one at 8.38 GHz and the other at 8.62 GHz. At −10 dB, the reflection bandwidth is 460 MHz, from 8.26 to 8.72 GHz. Two proposed filters show an insertion loss about −0.5 dB and −0.8 dB within the passband region. These filters show high out of band rejection in lower and higher frequency ranges. The first filter shows a transmission zero at

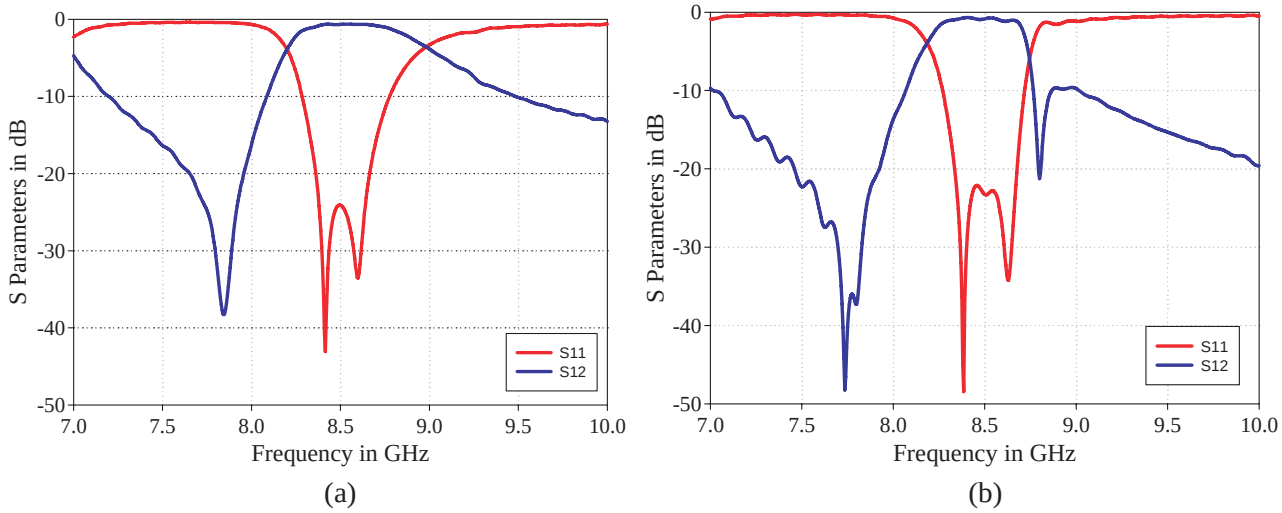


Figure 6. (a) S_{11} and S_{12} of filter with single CSRR. (b) S_{11} and S_{12} of filter with two CSRR.

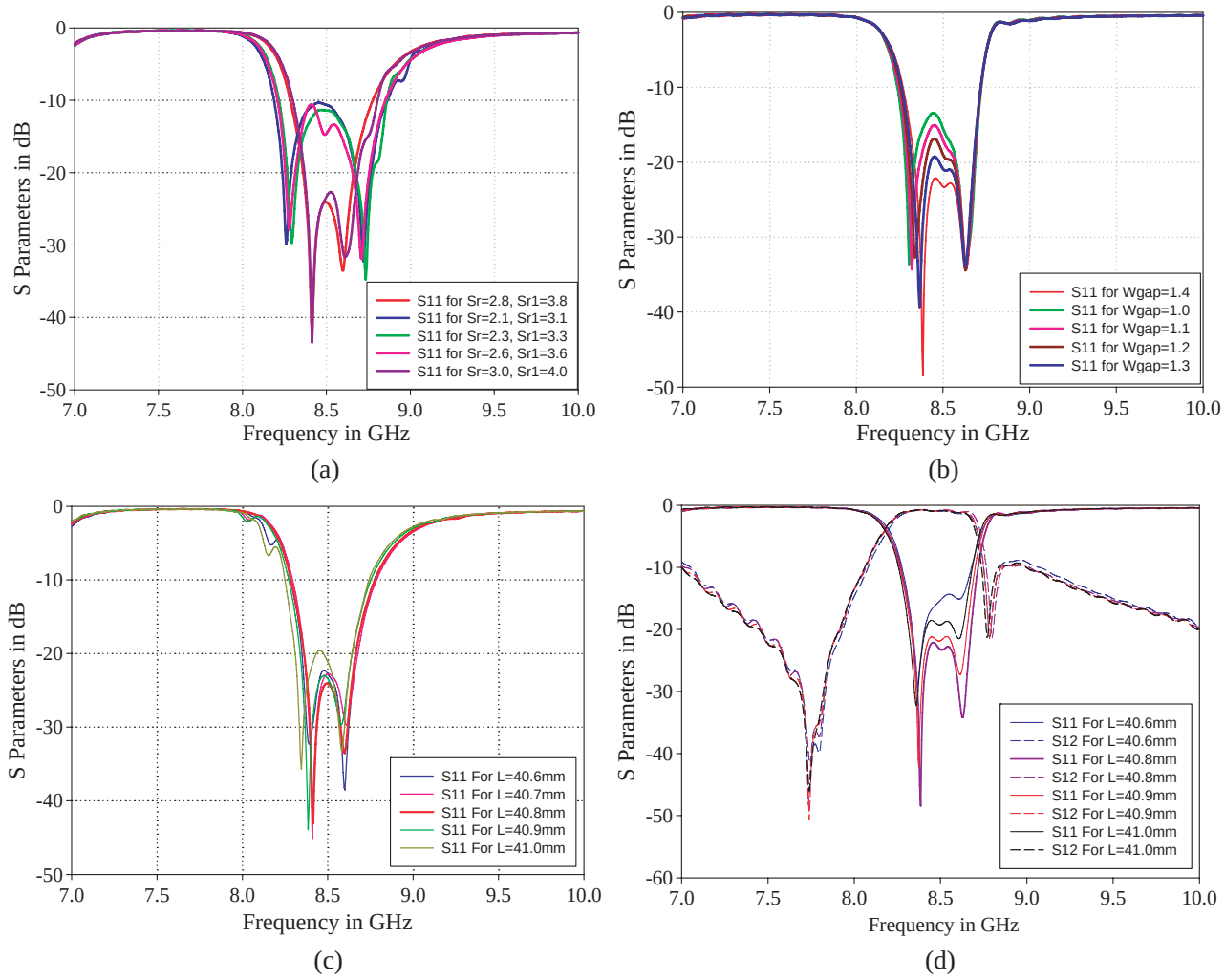


Figure 7. (a) parametric response w.r.t S_r and S_{r1}. (b) Parametric response w.r.t W_{gap}. (c) & (d) Parametric response w.r.t L for both the filters.

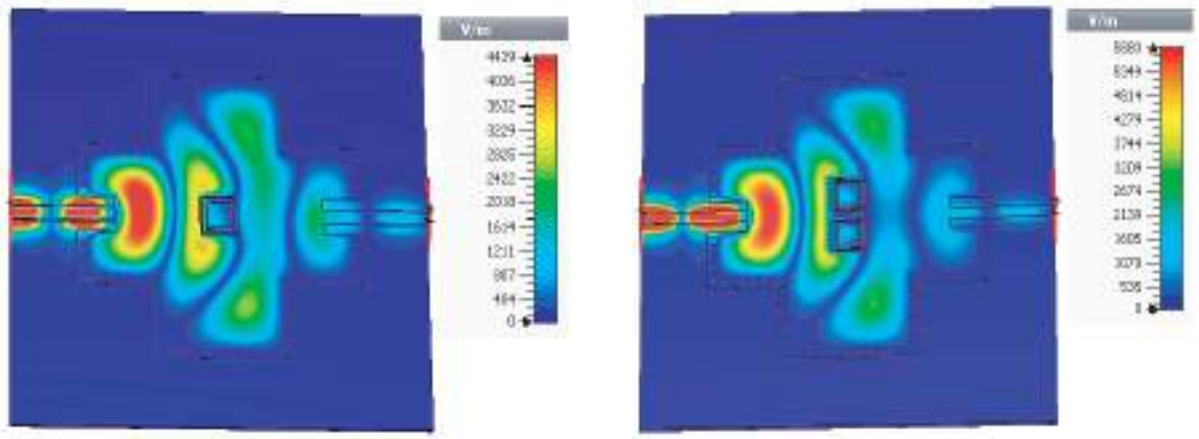
7.85 GHz which is introduced by single CSRR slot, and the second filter shows two transmission zeros at 7.73 GHz and 8.8 GHz, because of two CSRR slots. In order to increase the roll-off rate of the band pass filter, two CSRRs have been used instead of single CSRR.

4.1. Parametric Analysis

A set of training data required to train the neural network is generated from the parametric analysis of both the filters, and the corresponding parametric plots are depicted in Figure 7. This analysis was carried out by changing different parameters of these filters like S_r, S_{r1}, W_{gap}, and L.

4.2. E-Field Distribution

Figures 8(a) and 8(b) show the electric field distribution of filters with single CSRR and two CSRRs, respectively. The electric field strength of the proposed filters is indicated by the vertical colour ramps (right side of Figures 8(a) and 8(b)). The red colour shifts on the upper surface of the filters represent the growth of the electric field strength. The proposed CSRRs incorporated SIW filters show the TE_{10} (dominant mode) behaviour like conventional rectangular waveguide.



(a) (b)

Figure 8. (a) Electric field distribution of filter with single CSRR. (b) Electric field distribution of filter with two CSRRs.

5. FABRICATION AND PRACTICAL VALIDATION

The proposed filters are fabricated, and the top views of the two prototype models are shown in Figures 9(a)–9(b), and the back view is shown in Figure 9(c) with dimensions mentioned above. Rogers RO4003C is used as the dielectric substrate with a relative permittivity of $\varepsilon_r = 3.55$ and loss tangent of $\tan\delta = 0.0027$, and the height of the substrate is $h = 0.81$ mm. The fabrication was done by using the standard PCB process. At the initial stage of fabrication, copper metal is used to coat either side of the substrate material. Vias are drilled in order to form the SIW structure, and these vias are coated with copper metal. In the final stage of fabrication, the CSRR slots are etched on the upper PEC as shown in Figure 9. The measurement of prototype models is carried out with the help of Combinational Analyzer (Anritsu-MS2037C), and the measurement setup is shown in Figure 10.

The measured results are compared with the simulated ones as shown in Figure 11, and they are in good agreement. From Figure 11(a) and Figure 11(b), at -10 dB it is observed that the measured S_{11} is shifted by 50 MHz (from 8.28 to 8.33 GHz) and 70 MHz (from 8.26 to 8.33 GHz) respectively from simulated S_{11}, and at the centre frequency (8.5 GHz), measured S_{12} is shifted by 0.41 dB and 1 dB respectively from the simulated S_{12}. The slight mismatch in results is due to the fabrication tolerances, and this deviation is also because SMA connecters are not taken into account while the simulation is

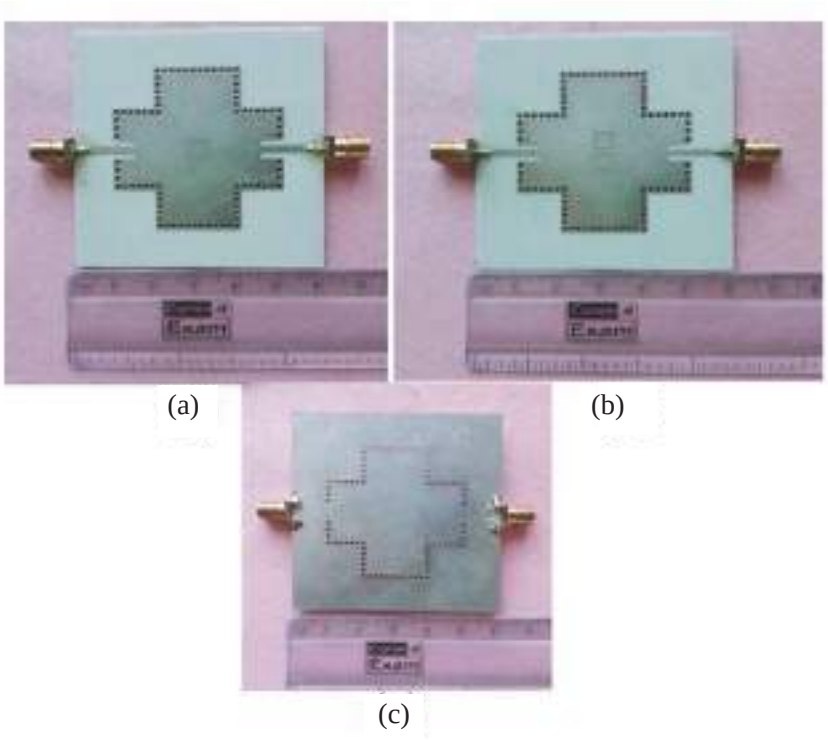


Figure 9. Fabrication models of SIW BPF. (a) With single CSRR. (b) With two CSRRs. (c) Back view.

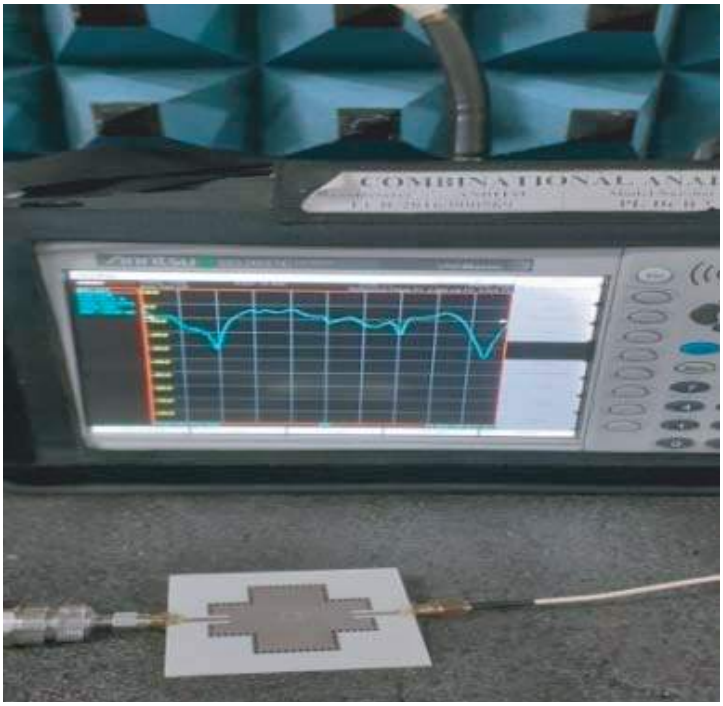


Figure 10. Measurement setup.

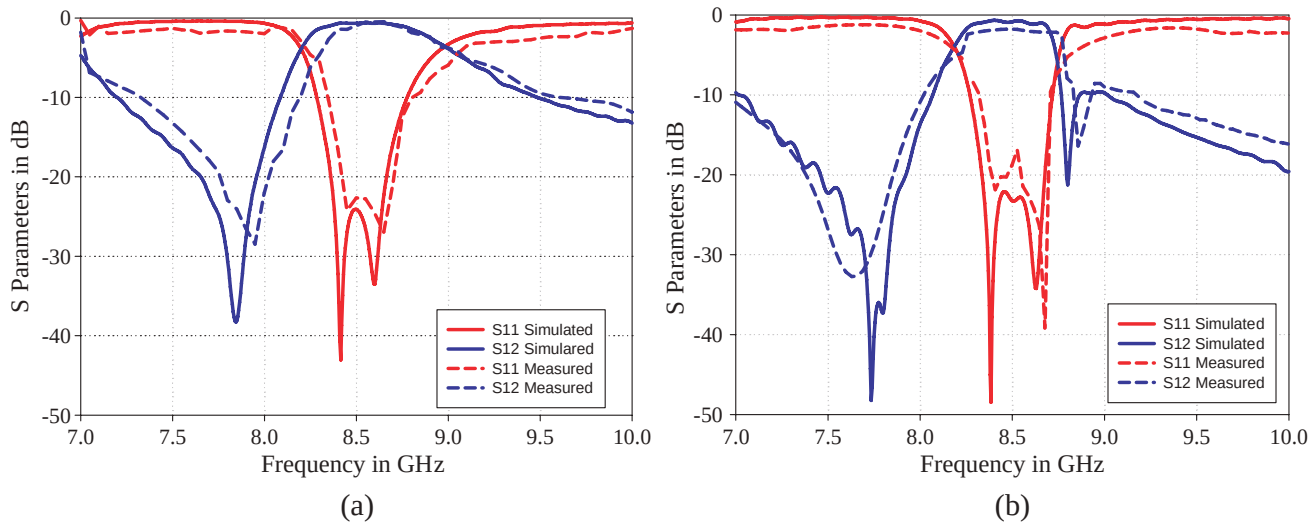


Figure 11. Simulated and Measured results of (a) BPF with single CSRR, (b) BPF with two CSRRs.

performed. At the passband centre frequency, the two results show better than −22 dB and −18 dB return losses, respectively.

The performance parameters of the proposed bandpass filters, such as passband center frequency, insertion loss, fractional bandwidth, return loss, dielectric substrate, and type of technique used have been compared with the previous literature and are summarized in Table 5. From Table 5 it is clear that the proposed filters provide better insertion loss, fractional bandwidth, and return loss.

Table 5. Comparison of proposed filters with similar bandpass filters.

Ref. No.	f_0 (GHz)	IL (dB)	FBW (%)	S_{11} (dB)	Substrate (ε_r)	Technique
[15]	3.5	1.45	6	−20	Taconic RF-30(3)	CSRR
[19]	5	≈ 2	3.2	−16.6	Roggers RT Duroid 5880(2.2)	CSRR
[23]	2.4	1.25	10.5	−20	Roggers RO4003C(3.55)	FOCSRR
[24]	5.8	0.9	8.5	−22	Roggers RT Duroid 5880(2.2)	CORR
[25] (Measured)	15	1.7	4.3	≈ −20	Roggers RT Duroid 5880(2.2)	—-
This work Filter I	8.5	0.5	8.5	−24	Roggers RO4003C(3.55)	CSRR, ANN
Filter II	8.5	0.8	6.1	−23	Roggers RO4003C(3.55)	CSRR, ANN

f_0 = Pass band center frequency; IL = Insertion Loss; FBW = Fractional bandwidth.
Filter I: SIW bandpass filter with single CSRR
Filter II: SIW bandpass filter with two CSRRs

6. CONCLUSION

Two bandpass filters based on SIW with CSRRs are implemented with the help of an FF-MLP neural network. The neural network is trained properly, and the parameters S_r, S_{r1}, and W_{gap} are optimized. The prototypes of proposed filter configurations are fabricated using PCB combined with plated through hole technology, and the measured results are in good agreement with the simulated results and neural network optimized results. The measured reflection coefficients for the two filters are -22 dB and -18 dB, respectively, and the insertion losses are -1 dB and -3 dB, respectively. The computational time of the neural network is very low compared to the full wave simulations performed with CST microwave studio. The mean square error measured between simulated and neural network results is almost negligible. Hence, the FF-MLP neural network with LM algorithm is one of the best parameter optimization techniques, compared to other commercial software.

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TUMOR DETECTION IN SKIN USING ELECTROMAGNETIC BAND GAP STRUCTURE ANTENNA

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Abstract - *Tumor in skin could lead to death if not taken proper attention. Sometimes it may lead to most serious situations like skin cancer, which is Glioblastoma. The death rate is about 0.7 in last 2 years due to delay in the diagnosis. This distributed nature of the cancer also made this challenge in the treatment and diagnosis of the tumor or cancer in the skin muscles. Imaging techniques are traditionally used in detection of tumor in skin. Another approach is by using RF reflection approach, in which detect of tumor in skin done by analyzing variations in received signals from the skin model with and without tumor. So, in this work a EBG based monopole patch of circular shape with rectangular slot antenna is proposed that can detect the cancer related tumors in skin. The patch is pasted in the economical dielectric substrate Polymide. The design has its dimensions of 35 × 35 × 1.5 mm³ and that can radiate with a maximum gain if 1.12 at ISM 2.4GHz with 0.3519 GHz bandwidth from 2.2987 to 2.6506 GHz. The radiating efficiency of antenna is 65.3%.*

Keywords: Monopole Antenna, Skin Tumor, Monostatic Radar and radiation efficiency.

1. INTRODUCTION

In nature there are many health issued that cause human that, in which caner is one which causes significantly high death rates. This is happened due to late identification and also lack of self confidence [1-2]. There is high possibility of increasing patient life time, and sometimes cured if it identified in early stages like first and second stage. The many imaging techniques such as PET-CT (Positron Emission Tomography scan, Computed Tomography), Magnetic Resonance Imaging (MRI), Electro Encephalography (EEG), Magneto Encephalography (MEG), Magnetic Induction Tomography (MIT), and Electrical Impedance Tomography Technique (EIT) etc., are used in the detection of suspected tumors. But these methods require pre medical preparation of patient and need of experience doctor's observation. The process is time taking and costly. And also the results are not obtained instantly. So latest investigations in RF engineering is made to support the bio medical application such as in detection of tumor cells in human body with less time and low cost.

In this sensor antenna plays a vital role. An impressive flexible antenna that used to detect various glands based on Electromagnetic Impedance Tomography technique using microwave frequency to detect tumor [3-4]. There are various works made bay changing substrate properties like Giigml1032, FR4, Taconic (TLY-5) substrate etc., and obtained satisfactory results detection of breast cancer in [5-8]. But the sizes are not comfort to patient to fit over breast. In [7] smart antenna using PCA and LDA classification algorithms also applied to differentiate cancer tumors form normal glands. Some works used the Inverse Fast Fourier Transform (IFFT) for spectral analysis to filter out the noise for accurate results. An antenna array is proposed in[10] to detect tumor, that is fabricated on PET substrate. A polyester based antenna array and skin wearable array antenna for skin tumor detection is proposed by Alqadami et.al, it has multilayer and large size. [11-12]. The detection is done by imaging system. Compact a conformal antennas are also used based on EMIT technique to detect tumors.

From above literature, a pentagon slotted disc monopole antenna is proposed in this work. The proposed design is patched on 1.6 mm FR4 substrate with dielectric constant of 4.4. The article is organized to four sections. Section I includes introduction along with literature, the patch antenna design geometry is discussed in section II, Human skin modeling using CST values covered in Section III, results and discussion are in Section IV, and finally Section V concludes the work. The design made to radiate at ISM 2.4 GHz band. Design and simulation is done using CST studio software and results are recorded.

The proposed circular patch micro strip antenna is constructed by three layers; they are ground layer, substrate and patch. Here the shape of patch is considered as circular. The substrate material is Polymide dielectric material and the properties of this material are noted as: height is 1.5 mm, dielectric constant of 3.5 and 0.0025 loss tangent. The micro strip line method is used to provide the excitation. The dimensions of substrate is 35 x 35 x1.5 mm³ and this is the size of proposed antenna. length of the feed line 17.134 mm, and width of the feed line 4.4 mm.

A reactangular shape of slot is introduced in a circular patch. In this the ground is removed till the feed line that allows radiation in the desired ISM band frequency. The finalized design shown in Figure 1 is obtained by number of approximation using the software and the final design metrics of proposed antenna are listed in Table 1.

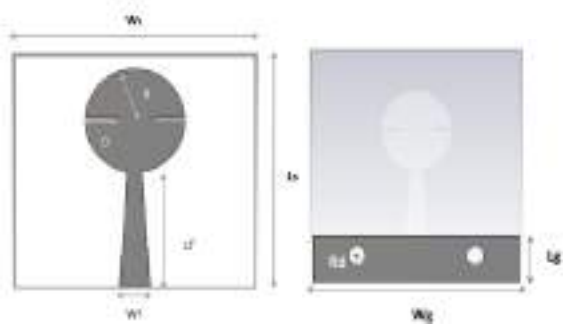

Figure 1: Design Model of the proposed antenna

Table 1: Design parameters of the proposed antenna

Variable Name	Symbol	Unit (mm)
Width of substrate	Ws	35
Length of substrate	Ls	36
Width of the feeding line	W_f	4.4
Thickness of substrate	T	1.5
Length of feeding line	L_F	17.134
Radius of circular disc	R	6
Length of one side ground plane	L_G	5.9
Width of one side ground plane	W_G	35
Radius of EBG unit cell	Rd	1.5
Length of one side slot in patch	D	4.4
Width of one side slot in patch	D1	0.5

3. MODELING OF HUMAN SKIN

The proposed antenna is designed for detecting the stroke in human skin. The human skin models of three layers were created in CST MW Studio with the help of dielectric properties. The three layers of human skin model are skin, fat and bone. The dielectrical properties are dielectric constant and conductivity depending upon the size and thickness of layers. The Figure 2 shows the placement of antenna in front of human skin model. Then the antenna exhibits parameters like electric field, magnetic field, surface current and current density. These values are analyzed and then tumor of size 3 mm is placed on human skin model.

The same antenna parameters are analyzed and compared with previous parameters of antenna. The figure 3 shows the human skin mode with tumor model.

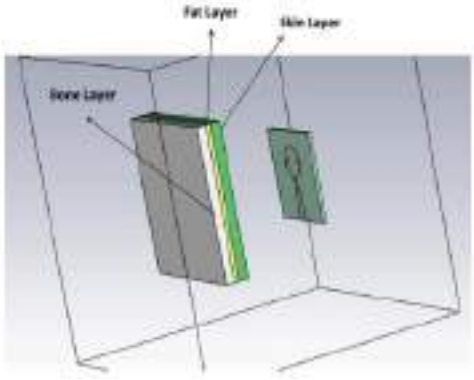

Figure 2: The positioning of proposed antenna in front human skin model in CST MWS

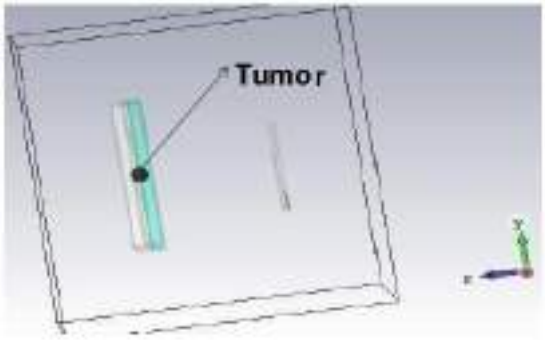

Figure 3: The spherical shape of tumor is introduce in human skin in CST MWS

Table 2: Human skin and tumor model

Skin model	Depth of layer (mm)	ε_r	σ (S/m²)
Skin (Dry)	2	38	1.5
Fat	2	5.3	0.1
Muscle	4	53.5	1.8

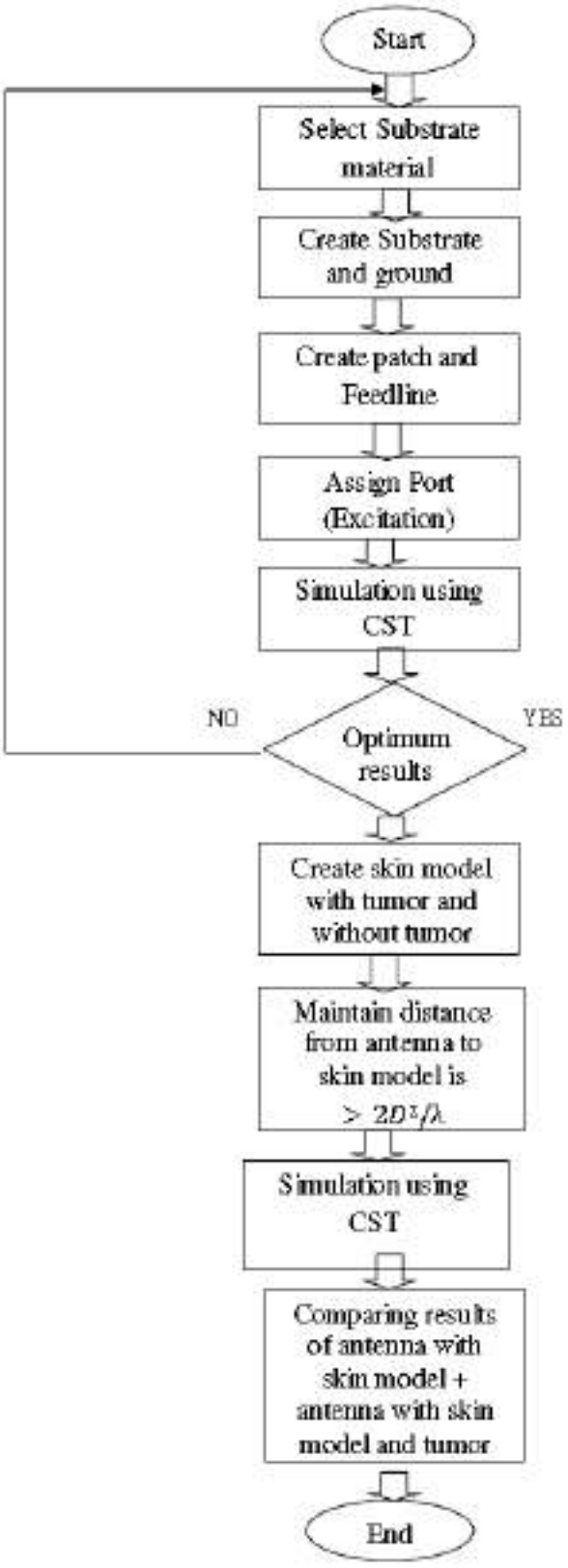

Figure 4: Flow chart of proposed design

4. RESULTS AND DISCUSSION

The simulation results of proposed micro strip patch antenna shown in figure 4. By observing the S-parameters graph(return loss Vs Frequency), the proposed antenna operate at 2.45 GHz frequency and it provide band width 351.9 MHz at -10 db return loss and reflection coefficient is -15.265. An efficiency of 63.5% and gain is 1.12 dB in a normal position for proposed circular patch antenna which is being simulated in free space.

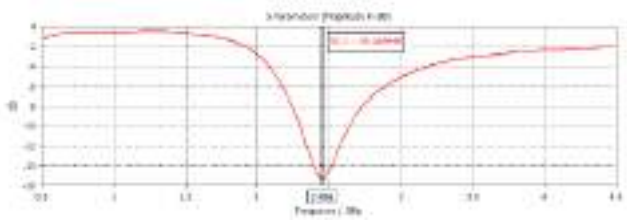

Figure 5: S-parameter plot for the proposed micro strip patch antenna

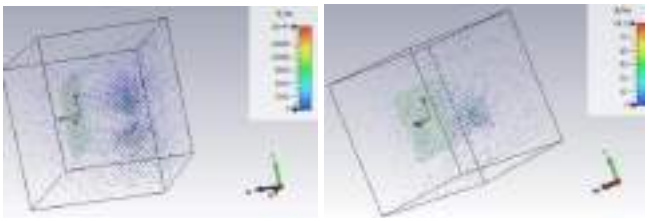

Figure 6: Electric and Magnetic Field values of the proposed antenna with skin model in CST MWS

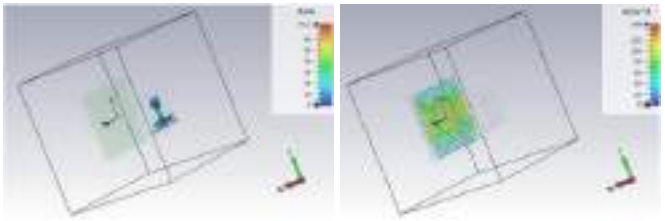

Figure 7: Surface current and current density values of the proposed antenna with skin model in CST MWS

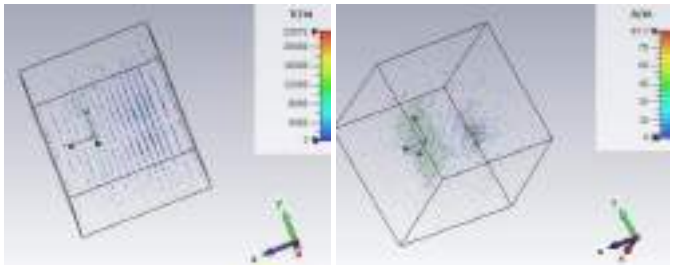

Figure 8: Electric and Magnetic Field values of the proposed antenna with skin model and tumor in CST MWS

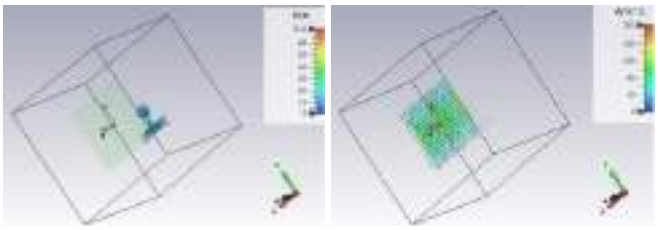

Figure 9: Surface current and current density values of the proposed antenna with skin model and tumor in CST MWS

Table 3: The result comparison among the proposed antenna without tumor and with tumor

	Electric Field (V/m)	Magnetic Field (A/m)	Surface current (A/m)	current density (A/m^2)
For proposed antenna with skin model without tumor	**18744**	**89.5**	**73.1**	**148**
For proposed antenna with skin model and tumor	**23072**	**87.7**	**71.6**	**203**

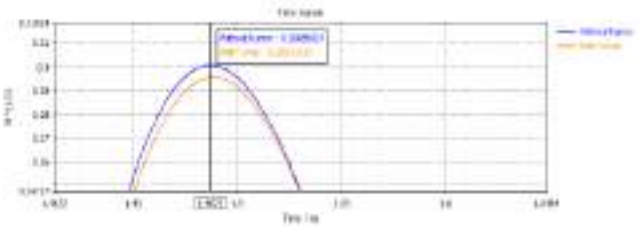

Figure 10: Amplitude Variation between Reflected signals with and without tumor model

Table 3 shows the comparison of antenna parameters among the proposed antenna without tumor and with tumor. From the above table, electric field, magnetic field, surface current and current density values for without tumor and with tumor are varied, with help these threshold values and also using the variation in Reflected signals with and without tumor model (shown in figure 9), the proposed circular patch antenna able to detect tumor in skin.

5. CONCLUSION AND FUTURE SCOPE

In this article a rectangular slotted and circular shaped microstrip patch is proposed for tumor tissue detection in skin that can radiate 2.4 GHz. It has significant radiation band from 2.2987 to 2.6506 GHz) allows S and applications along with ISM 2.4GHz band. Removal of complete ground gives the radiation similar to monopole. The slot provided in the patch makes the patch radiate at low frequencies, so one can treat it as electrically small antenna. The size 35 × 35 × 1.5 mm^3 shows compactness and easy to use with patient. More accuracy can be obtained by using a group of such pact antennas by forming a curved shape to suit the skin structure.

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Intelligent High Tech Street Lightning Pole for Smart City

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ABSTRACT

The alarming increase in energy price and maintenance cost results in significant increase in lighting budgets. With Smart Street lights, cities can save energy and minimize CO_2 emissions, limit light pollution & minimizes maintenance cost. Street light is the basic infrastructure of a city. Utilization of Sensors for data collection in Street light becomes the basic design of a Smart City. Smart Street light provide secure traffic situations and secure pedestrian environment resulting in better infrastructural improvement to Smart cities. The article elaborates on the design of Intelligent Street lightning pole towards energy efficient lightning management services and other emergency handling facilities. The features of the design covers to way finding, business advertisement, weather station, rain and flood monitoring and so on.

Keywords
Smart city;Secure solution;Intelligent street light; Light pole;Energy saving;Light pollution;EV charging;Embedded

Introduction

Street Light [1] plays a major role in current smart cities. Street light is the primary source of light on road and located in the intersections of roads. In majority of locations, traditional street lights are used, which uses heavy materials & more power. In current scenario of cost hike in materials & various social responsiveness to issues in environment leads to identifying the alternative technologies to save power and cost. LED Street lightning answers the issue towards environment friendly & reduction in cost. With the utilization of Embedded Sensors & Digital Networks, they gather and transfer data which help to monitor cities and respond to any situations. Intelligent Street lightning system can detect bottleneck in traffic and detects the vacant parking slots. Also, the networks can minimize the energy consumption by controlling the LED lights remotely to turn off and on, flash and dim. Smart lightning system results in saving energy, minimizing cost, reduction in maintenance and CO_2 emissions. The intelligent Street lightning [3-5] can be made as Smart Poles also, which caters combined smart services & amplify the business potentials. The Smart pole can cater as infrastructure for 5G, Wi-Fi hotspots, Surveillance cameras, Environmental sensors and Electric vehicle charging points.

The 3 significant force in developing the smart street lightning are regulatory policies, Internet of Things (IoT) convergence and LED prices drop [1].Figure 1 shows the key market drivers of smart street lightning. Across Globe, 320 million street lightning poles are present with Asia possessing 25%, North America and Europe 20% and South America for 10%. Figure 2 displays the top 10 cities implementing connected streetlights. Street lightning infrastructure has three potential parameters towards smart cities implementation comprising capillarity, electrification and connectivity. Smart Cities [6] uses various sensors, information technologies aligning with IoT to collect and supply from city infrastructure [2].Smart city results in more accessible, cleaner, healthier, safer and pleasant for its residents. Figure 3 displays the smart city components comprising home, transportation & mobility, farming, mobile payments and various other services.

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Figure 1. Key Market drivers of Smart Street Lightning

Figure 2. Key Market drivers of Smart Street Lightning

Figure 3. Smart City Components

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Literature Review

B.C.Mishra [7], et al described that using Zigbee based Wireless devices optimization done in efficiency of street lighting systems. Using Embedded Internet Technology, a monitoring system design done for Street light. The results proves that the proposed system solves various essential applications such as street light management, real time access and so on pertaining to Embedded Internet applications.Eungha Kim[8], et al described a methodology where people can control certain devices utilizing Internet services in Smart Home. It proposes an integrated community service platform system architecture which provides solution for Smart city/home using a single integrated and intelligent community services.M.K.Sheu [9], et al, describes about Smart Street light which results in road safety and energy saving. Embedded System monitors the status of road and output control instruction. Low color temperature light is generated by embedded system when fog or rain is detected. Proposed LED Street light results in better ambience of intelligent city by improving the road safety for pedestrian and driver.E.Kougianos[10], et al, described that the Image or Video exchanges over the IoT is a requirement in various applications such as smart structures, intelligent health care and smart city planning.

A.Murtuza [11], et al, proposed a system which detects presence of vehicle for a certain distance and the light gets switched on during the vehicle passing the defined radius. Also, a prototype is incorporated to intimate the defect in street light if any identified. The proposed system results in consumption of power and also uses solar energy during day period. Also, the system elaborates on the minimum utilization of manpower for detecting the faulty street lights and intimation to the substation.S.Arslan [12], et al, discusses about significant application of IoT in designing a smart city for street lightning system. The designed system operates on the principle Light Dependent Resistor (LDR) which operates the bulb depending on the light intensity. Also, the discussed system is designed at economical prize with inclusion of various sensors to measure the atmospheric parameters with the aid of Android [20] operating system for effective utilization.N.Ouerhani [13], et al, elaborates on real time solution for street light control and utilization of IoT system. The design results in energy saving with respect to traditional street light control system.

M.S.A.Muthanna [14], et al, elucidates on the implementation concept of Smart City using a Wireless technology which caters long range and consumes low about power named LoRa. The system discusses with smart street lightning including the overall network organization with logical implementation. D.VijendraBabu [15], et al, discusses remote street light monitoring and controlled system. It results in conservation of power with the use of PIC Microcontroller.
Y.Yang [16], et al, proposes about efficient system for street light and utilization of sensors included to obtain the interface of data collection. The system details about Edge Computing services with high commercial value.RishikeshLohote [17], et al, exposes the conventional usage of Street lightning which results in wastage of electricity between 20 to 40% & proposed usage of Smart street light lamps which results in energy efficiency and assists in displaying various significant parameters such as weather forecast, water level sensor alerts & emergency notifications overcoming the drawbacks of conventional street light system.

Yoo S Song [18], et al, elaborates on smart lamppost composing of intelligent edge unit, camera, short range communication device, digital signage, etc. One of the main functions in the smart lamppost is to forward the safety information to the gateway node by an I2I communication system. The article analyses on the latency and throughput at each node during multi-hop data transmission to the gateway node.GunjanBhartiya [19], et al, elaborates on intelligent lightning control and energy management system. It describes about designing an efficient energy saving mechanism using microcontroller and sensors which turn on/off street lights automatically which results in energy consumption with the utilization of sensors.M.Suresh [20], et al, elaborates on utilization of reliable smart management proposal for minimizing the wastage of power in street light with the utilization of Wi-Fi module, Light Dependent Resistor (LDR), accelerometer and ultrasonic sensors are employed. Intelligent lightning control and energy management system. A Predictive model based on Improved Bayesian Neural Network (IBNN) model is applied which eliminates the power wastage during night time if there is no vehicle or trespassers passing.

System Design

The purpose is to design an Intelligent High Tech Street lighting pole which runs an embedded web server for Smart Web based services in addition to the energy efficient lighting management services and other emergency handling

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facilities.The Block diagram displayed in Fig.4 and proposed Street Lightening pole sample is displayed in Fig. 5.STM32F429, Cortex-M4F Microcontroller [21-27] is used.

Figure 4. Prototype Block Diagram

Figure 5. Proposed Street Lightning Pole

Atollic True STUDIO & ST-Link Debugger tools are used. The Street pole consists of various sensors, Transceivers,

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Camera, LED Lights and connected to server. The unique features of the design are as follows

- Business advertising
- Weather station
- Rain and flood Monitoring
- Way Finding
- RGB LED light
- Festival lighting
- IP Surveillance Camera

Figure 6. Features of Intelligent Street Pole

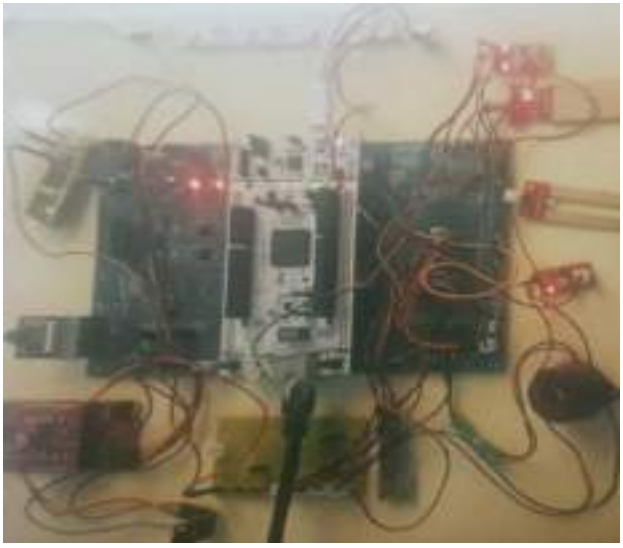

Figure 7. Snapshot of Hardware Module

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Fig.5 displays the proposed Lightning pole consisting of Wireless dual band mesh Transceiver, Smart grid lightning, Image sensors, Digital street sign & Signage, Concealed placement speaker, Dynamic lightning, Environmental sensors & emergency call station.Fig.6 displays features of Intelligent Street Light Pole which consists of Sensors, Video monitoring, RFID, Wireless network, Intelligent lightning, Information display & charging pile. The snapshot of Hardware module is displayed in Fig. 7.

Results & Discussions

IP Surveillance camera helps in monitoring the street continuously, which helps in assisting the theft/robbery incidents if happens. The Way finding is used to determine the correct path. Weather parameters such as Pressure and Temperature are measured continuously and uploads to the Internet. Using Festival lightning mode, the color of the Street light can be varied to fit with the festival conditions. Emergency speaker provides mass notification services during an emergency situations. Using Photocell control, the Street light is automatically turned on and turned off depending upon the circumstances. The Street lightning pole can also be used for business advertising resulting in revenue generation for authorities.Fig.8 displays the snapshot of result which displays the various modules/features listed in intelligent street lightning system.

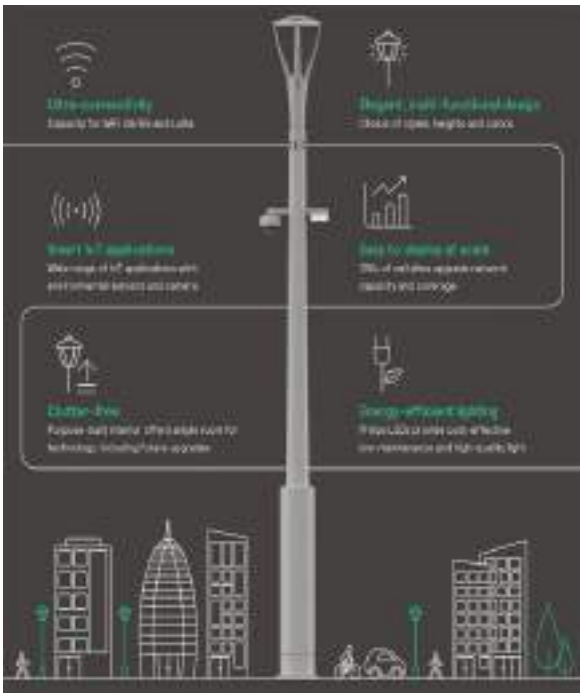

Figure 8. Intelligent Street Light

Conclusion

The article describes the concepts of an Intelligent High Tech Street Lighting Pole which caters the additional services along with essential services which runs on an Embedded Web Server This smart lighting system can be implemented in smart cities, parks, schools, educational institutions and common venues. It provides opportunity for revenue generation too & helps in emergency situations. Smart City journey starts with Smart Street lights which connects over 300-410 million streetlights worldwide with access with 24/7.The future ready systems becomes an open architecture with interconnected applications such as Traffic systems, Security systems, Environmental sensors, Weather systems,Emergeny response, EV charging,etc.The overall result in implementing Intelligent Street Lightning results in Adequate Light always, Optimization of Operation & Maintenance, Increased Public Safety, Minimization of Environmental impact, Secure Data connection & Globally compatible.

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Performance Analysis and Development Of Printed Circuit Microstrip Patch Antenna with Proximity Coupled Feed at 4.3 GHz (C-band) with Linear Polarization for Altimeter Application

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Abstract: This paper aims at design, develop, optimize and realize a printed circuit Microstrip patch antenna at 4.3 GHz (C-band) with Linear polarization for Altimeter Application with proximity coupled feed method. Antenna is a device which acts as a transducer converting electrical signal to electromagnetic wave and vice-versa during transmission and reception respectively. Development, optimization and testing of high performance Microstrip antenna working in C-band are carried out for Altimeter applications. Various types of antennas are available to meet these requirements. Among these, the printed circuit Microstrip antennas have gained great prominence. With modern wireless method of contact the basic antenna requirements are Gain, Bandwidth, polarization, Size must be low, weight must be low, ease of fabrication. All the requirements mentioned above could be done with the help of printed circuit antennas. Patch antenna is resonant style radiator having narrow bandwidth. Because of its narrow bandwidth this antenna tends to be more efficient and also it tends to be smaller in size which allows the use of this element in antenna arrays and helps in good control of radiation performance. In this project, first we design patch antenna with some design equations and model it in HFSS software.. The simulated results obtained from software are compared with tested fabricated results.

Keywords: Antenna, Gain, Microstrip Patch Antenna, Return Loss , VSWR, Return loss.

1. INTRODUCTION

Webster's dictionary defines an antenna as a "normally metallic structure" designed to radiate or absorb radio waves as a rod or cord. An antenna is a device that provides radio wave propagation or receives radio waves. The transformation from a directed wave to a transmit line wave called "Free Space" provides a different term [1].. It is an information instrument that converts EM photons into circuit current and can convert energy into photons which are radiated in space. For Radar Altimeter (RA) applications, Microstrip Antenna (MSA) operating in a C-band is performed [2]. In the previous forty years, the information paces of optical correspondence frameworks have encountered a bewildering increment from 100 Mbit/s per fiber during the 1970s to 10 Tbit/s in current business frameworks [3]. As of now, more than 95% of advanced information traffic is continued optical fiber organizations, which structure a significant piece of the public and worldwide correspondence framework [4]. To meet these requirements there are numerous types of antennas available. The MSA printed circuit has gained considerable popularity among these. Gain, bandwidth, polarization, size must be medium, weight must be medium, ease of fabrication are the basic antenna specifications of modern wireless method of communication. Most of them, however, are not workable or impractical. Compact MSA has been developed for RA applications at operating frequencies from 3.98 to 4.47 GHz. But antenna production was not examined [5]. MSA with I slot was designed and simulated at 4.5GHz. The results shown are not very promising and can hardly be feasible [6]. Antenna is designed to work within 4.3 GHz. Designed antenna is unfeasible and have not been analyzed for practical applications [7]. An array MSA with 2x2 configurations has been simulated and measured for RA which makes the design complex because of array

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of antennas [8]. The practical results are not embedded and will not be useful for communication applications [9]. Double L-probe fed for RA applications is developed in [10] at 4.3 GHz and a gain of about 5.95 dB is observed.

Radar Altimeter (RA) is a device that is used to measure a low altitude or elevation from an aircraft or a satellite to land or sea level. With the theory of radar, a vertical distance in an aircraft from the terrain just below it can be determined with an altimeter. Radio altimeter is a member of the radar [5-10]. With the support of printed circuit antennas any of the above requirements could be done. The fundamental theory of radar is that radio waves are transmitted to land or sea level and receive an echo signal for a long time.

Fig 1. depicts the schematic of MSA. It consists of ground plane at the bottom, a dielectric substrate of height h and a patch built on the substrate. Dimensions of ground plane are greater than substrate and patch [11].

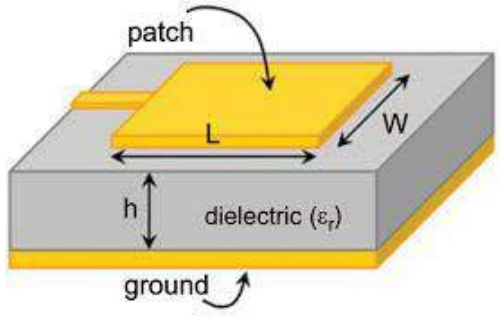

Figure 1. Microstrip Patch design

For the design of antenna, finding the parameters are essential. Important parameters are described below.

A. Radiation Pattern and HPBW

An antenna radiation is defined as "a graphic representation of the antenna's radiation properties as function of the space coordinates. The reflection coefficient is measured in the field region for certain instances and is perceived as a feature of the directional coordinates. It provides information on the antenna beam diameter, antenna side lobes. The most functional antenna designs include a main lobe and many secondary lobes which are called side lobes. The width of half the Power Beam "HPBW" is the same division in which the scale of the geometry of the radiation reduces by half (or-3 dB) from the peak of the main beam [12, 13].

B. Voltage Standing Wave Ratio (VSWR)

When reflection occurs in an incorrectly terminated line, voltage and power vary in magnitude along its length. When the transmission line is not terminated correctly, at the termination, the electromagnetic wave traveling from the generator at end of the line reflected in whole or in part. The standing wave ratio may be defined as the ratio of maximum to minimum current or voltage on a line having Voltage Standing Waves and this Ratio is abbreviated (VSWR) [14, 15].
Thus,

$$VSWR = \left| \frac{V_{\max}}{V_{\min}} \right| \tag{1}$$

Relation between VSWR (S) and Reflection coefficient (Γ):

$$VSWR = \left| \frac{V_{\max}}{V_{\min}} \right| = \frac{1+\rho}{1-\rho} \tag{2}$$

C. Return Loss

This is the best and most convenient method for estimating the sources of signal input and output. If the other end is not balanced the power returned is Return Loss [16]. In dB it is given as

$$RL = -20 \log |\Gamma| \text{ dB} \tag{3}$$

$$\Gamma = \frac{V_o^+}{V_o^-} = \frac{Z_L - Z_o}{Z_L - Z_o} \tag{4}$$

Where,

Γ = Reflection coefficient.
Vo^+=Incident voltage.
Vo^- = Reflected voltage.
Z_L and Z_o are the load and characteristic impedance.

D. Gain

Gain of antenna is the capacity of antenna to focus emanated power in proper direction [17].

2. METHODOLOGY

A patch antenna (PA) consists of a conductive layer of one side of the dielectric substratum and the opposite leg, covered by certain planar arrangement ground line [18]. A variety of benefits including lightweight, low volume, low cost, planar configuration, integrated circuit performance, etc. Less profile antennas are needed for high-performance space craft, missile applications are restricted in size, weight, expense, strength, installation ease & aerodynamic profile. A feed line is used for arousing over or indirect interaction with the radiation. There are several different feeding methods, and four most common methods are the line Microstrip feed, Coaxial probing, Aperture coupling, Coupling of proximity [19, 20].

A. Coaxial Feeding

Coaxial feeding is a method of feeding during which the coaxial inner conductor is bound to the antenna's radiation field where as the external conductor is linked to basement as described in Fig. 2 [22, 23].

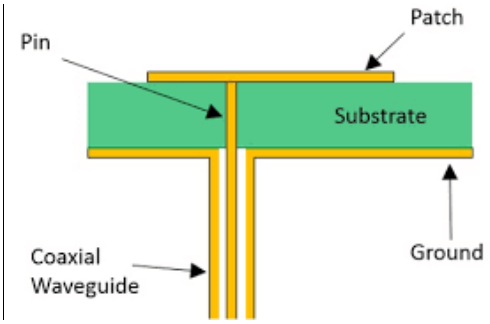

Figure 2. Coaxial Probe

The inner coaxial conductor is attached to a patch of radiation. The outer coaxial runner fits in to the ground plane. Has low spurious radiation. Its bandwidth is narrow. Particularly for thick substrates this is a difficult model (h>0.02>0).

B. Proximity Coupling(PC)

Low PC is used for high bandwidth and radiation, as defined in Fig. 3. However it is difficult to manufacture [21]. It has the highest bandwidth (as much as 13 per cent). It uses a two layer substrate.

1. Microstrip line→Lower layer.
2. Patch Antenna→ upper layer.

In this article, the results of the simulation are carried using HFSS software, and MSA is done using proximity-coupled feed method and both results are compared.

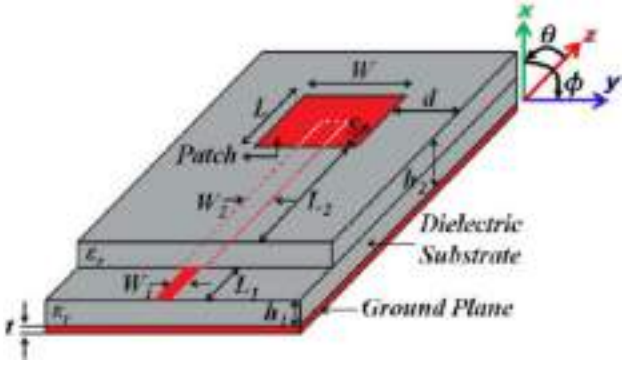

Figure 3. Proximity Coupling

C. Manual design calculations of MSPA

To design any MSPA, prior selection of few parameters is required. The design parameters of the proposed antenna are the operating frequency fr=4.3GHz, and RT / Duroid 5880 is taken as a dielectric substrate with di-electric constant of 2.20±0.02 and a normal factor for Dissipation is 0.0009[22, 23]. MSPA design parameters procedure is as follows

1) Width (W):

With the specifications including information about the ($\in_r$), (f_r), and (h). The procedure is as follows:
Equation 5 gives the width which provides efficient radiation.

$$W = \frac{c}{2 f_r}\left(\frac{\varepsilon_r + 1}{2}\right)^{\frac{-1}{2}} \quad (5)$$

For C=3*10^8 m/sec, f=4.3GHz, ε_r =2.2

Width calculated using above values is **W= 27.5 mm.**

2) Effective dielectric constant (ε_{eff}):

Find E_{eff} for MSA using equation 6

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{W}\right)^{\frac{-1}{2}} \quad (6)$$

Where, h = Height of the substrate.
W= 27.5 mm; ε_r = 2.2 ; h = 0.8 mm

Effective dielectric constant, calculated using above values is ε_r **= 2.116**

3) Extension length (ΔL):

Once W is found, determine the extension length ΔL (due to fringing effect) using equation 7.

$$\frac{\Delta l}{h} = 0.412\frac{\left(\varepsilon_{eff} + 0.3\right)\left(\frac{W}{h} + 0.264\right)}{\left(\varepsilon_{eff} - 0.258\right)\left(\frac{W}{h} + 0.8\right)} \quad (7)$$

Where, ε_{eff} = 2.116, h = 0.8 mm, W = 27.5 mm

Length extension calculated using above values **(ΔL)= 0.422** mm

4) Actual length (L):

The actual length of the patch can now be determined by equation 8

$$L = \frac{c}{2 f_r \sqrt{\varepsilon_{eff}}} - 2\Delta l \quad (8)$$

Where, f_r = 4.3 GHz, C = 3 *10^8 m/sec, ΔL= 0.422 mm, ε_{eff} = 2.116.

Actual length calculated using above values is L= 23.131 mm

5) Effective length (Leff):

The L_{eff} is found by using equation 9.

$$L_{eff} = L + \Delta L \quad (9)$$

By inserting values of L and Δl we get

L_{eff} =23.975mm

6) Ground Plane (GP) parameters:

Parameters are its length Ls and width Wg, which are two times of patch dimensions.

Ls=46 mm and Wg =56mm.

7) Microstrip line width (W_o):

The width of the microstrip line patch can be determined by equations 10, 11 and are given by,

$$Z_o = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W_0}{h}+1.393+0.667\ln\left\{\frac{W_0}{h}+1.414\right\}\right]}$$

for $\frac{W_0}{h} > 1$ (10)

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}}\ln\left[\frac{8h}{W_o}+\frac{W_o}{4h}\right] \qquad \text{for } \frac{W_o}{h} < 1 \qquad (11)$$

By trial and error method for Zc = 50 Ω. We get W_o as 2.06 mm. (~2.1) and $\frac{W_o}{h}$ = 2.625 thinner microstrip substrate results in less spurious radiation from feed lines, but higher loss. A compromise of 0.001λ to 0.002λ can be chosen for iterations. When the value is greater than 1, equation 10 can be used to get the value of Wo and is given by Wo=2.95mm. The wavelength equation is given by

$$\lambda = cf \qquad (12)$$

Where, C= 3*108 m/sec; f = 4.3 GHz = 4.3*109 Hz.

Wavelength λ=69.76m

8) Calculation of Microstrip length yo: (Distance from patch edge to position of feed):

In general, the conductance is given by,

Radiating Conductance, Gr = 1.7 X10 $^{-3}$

$$Z_c = \frac{1}{2(G_T)}\left[\cos^2\left(\frac{\pi}{2}y_0\right)\right] \qquad (13)$$

Where, Zc = 50Ω, Gr = 1.7 * 10^{-3}

From equation (13) the microstrip length is calculated and is given by microstrip length, **Yo = 8.77mm.** MSA designed values are calculated and are shown in table 2.

TABLE I. FINAL MSA DESIGNED VALUE

Parameter	***Value***
Length, L	23.13 mm
Width, W	27.5 mm
Microstrip Width, W_o	2.95 mm
Microstrip Length, Y_o	8.77 mm
GP length, L_g	46 mm
GP width, W_g	56 mm
Effective length, L_{eff}	23.975 mm
Effective dielectric constant, ε_{eff}	2.116
Wavelength, λ	69.76
Length extension, ΔL	0.422 mm
Radiating conductance, G_r	1.7 * 10^{-3}

3. SIMULATION OF MSA USING PROXIMITY COUPLED FEED METHOD USING HFSS

The Proximity feeding technique is chosen for successful impedance matching. In this case, a square micro stripe patch is used using 50-ohm probe feed. Altimeter's proximity feeding is best suited for fast mounting and it provides low cost and manufacturing flexibility.

HFSS is an immersive simulator, with tetrahedron as the base mesh part. This helps us to resolve some arbitrary 3D geometry, particularly those that use such techniques in a fraction of the time it would take for complicated curves and forms. Following steps are to be performed in the design of MSA MSPA modeling

A. MSPA modeling *using HFSS*

MSPA dimensions carried with HFSS involves following steps:

- The HFSS co-ordinates are designed or calculated using patch antenna dimensions.
- From the obtained coordinates at 3D proximity coupled microstrip patch is drawn as illustrated in Fig. 8.
- Mark, ground plane and microstrip feed are assigned as ideal material for electrical conductors, and RT/5880 is assigned to substrates.
- An air box "radiation box" is created around the patch and the boundary of the radiation is allocated to either side of the box.
- Wave port is assigned to the patch antenna for excitation purpose.

B. Optimization using HFSS

In HFSS Software, there are six optimization techniques

- Quasi Newton (Gradient) is being used to find the maximums and minimums of local features. These are based upon Newton 's principle, where a function point is 0.
- Pattern Search is a mathematical technique of optimisation that does not inherently require a gradient and is suitable for functions that are not continuous or differentiable.
- Genetic Algorithm (Random search) are used to produce high quality search optimization solutions using bio - inspired providers such as iteration, crossover and selection.

- Sequential Quadratic Programming "SQP" is iterative method of minimal, non-linear optimization. SQP approaches are used with a double continuous discrepancy between objective function and constraints in the context of mathematical problems.
- Sequential Mixed Integer discrete computing describes scalability problem with continuous and integer factors in the optimization area.
- Matlab is a computing environment designed for recursive design and operational processes is paired with a programming language that explicitly communicates mathematics in matrix and arrays.

If the buildup co-ordinates are defined in HFSS software, a 3D perspective on repairing and re-enacting to get different attributes. If the characteristic doesn't fit once with the anticipated, the patch and feed measurements differ in small steps and re-simulate until characteristics are necessary or obtained. Thus parameters such as feed duration under the patch, feed width, and patch length are optimized` directly without creating a handmade patch and then checking it with practical measuring techniques.

Therefore, the patch length is adjusted during optimization to suit the antenna requirements. During optimization to meet the antenna specifications, the patch length (mm) is optimized. Fig. 4 depicts 3D view of proximity coupled MSA and its view in HFSS is depicted in Fig 5.

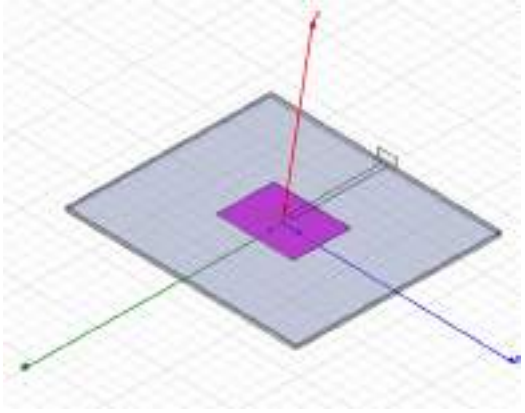

Figure 4. 3D view of Proximity Coupled

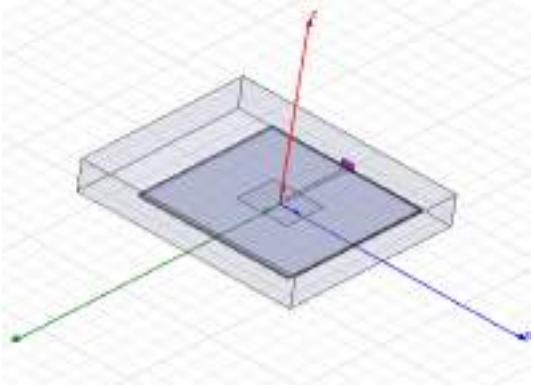

Figure 5. View of HFSS Model

C. Simulation

After the designing of the microstrip patch antenna the simulation is performed. Following steps are to be performed for the results in HFSS.

- After the design of MSA the simulation is performed.
- To view the errors and warnings, firstly validation is performed.
- Next, the set up is assigned to the antenna, which includes operating frequency 4.3 GHz, sweep in the range of 3.5 to 4.5 GHz. With step size of 0.1 GHz.
- Analyze all is selected to perform the simulation.
- Finally, the required antenna parameter graphs are observed in HFSS.

D. RL Graph (dB)

Fig 6 depicts the plot of RL(dB) and f(GHz)

E. VSWR Graph

From the plot as given in Fig. 7 the VSWR is minimum at resonant frequency 4.3 GHz. As, VSWR is approximately closer to 1, no signal is reflected back towards the feed i.e entire signal will be transmitted to the patch.

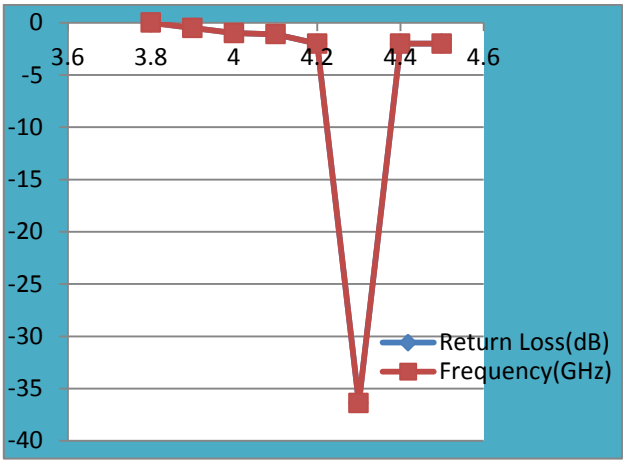

Figure 6. Return Loss (RL) (dB) plot

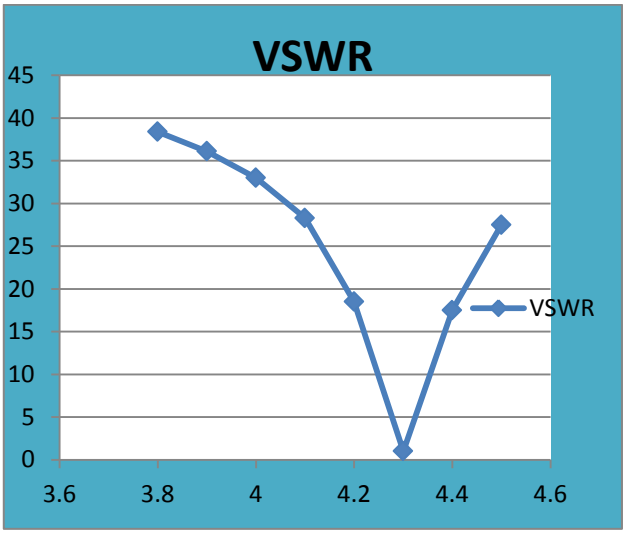

Figure 7. VSWR Graph

F. 2D Radiation Pattern Graph (Gain vs Theta, far field region)

The below graph shown in Fig. 8 is a 2D rectangular radiation plot observed in the far field region.

Figure 8. 2D Radiation Pattern Graph

G. Polar Radiation Pattern Graph

The below graph Fig. 9 is a polar radiation pattern plot.

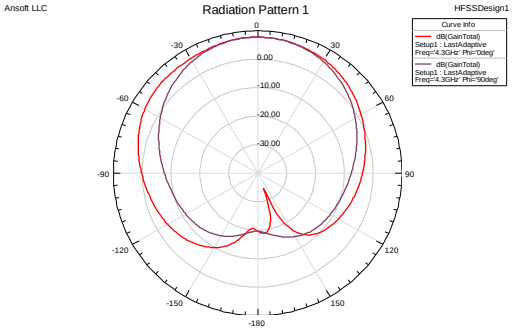

Figure 9. Polar Radiation Pattern Graph

H. 3D Polar Radiation Pattern Graph

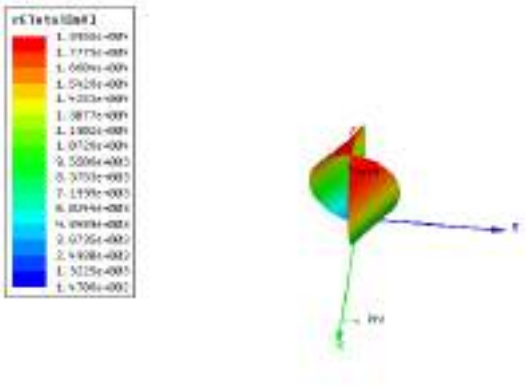

Figure 10. 3D Polar Radiation Pattern Plot

Fig. 10 is 3D polar radiation plot depicting the radiation intensity with respect to spherical coordinates is observed.

I. 2D Radiation Pattern Graph: (Gain vs Frequency)

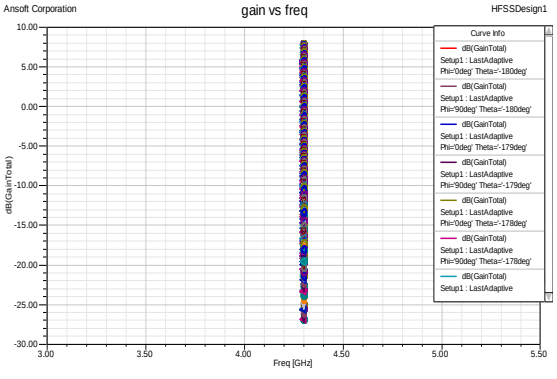

Figure 11. 2D radiation Pattern Plot (Gain vs Frequency)

The 2D Radiation pattern plot is shown in Fig 11. It will resonate at 4.3GHz.

4. FABRICATION AND TESTING OF ANTENNA

The design parameters specify all of the patch antenna measurements. Coordinates are obtained according to dimensions of antennas. The coordinates are the optimised to achieve the requirements of the given antenna using HFSS as described earlier. The results obtained by 95 per cent using HFSS correspond to the realistic results, so the coordinates can be fed directly to AutoCAD to generate the antenna layout. Fig.12 demonstrates the configuration of the patch Interface and MS feed section. Fig.13 displays the flowchart for measures involved in the manufacture of patch antennas.

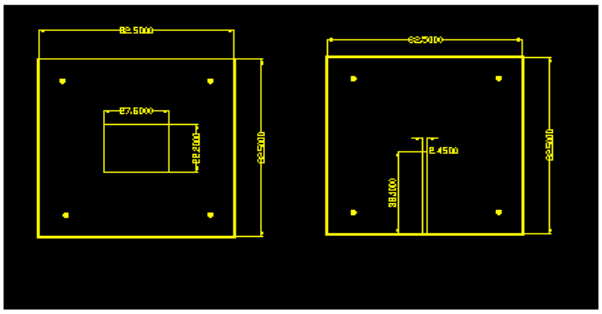

Figure 12. Patch Layout and Microstrip Feed line Layout

A. *Selection of Substrate materials*

Substratum content determination plays a big job in organizing the Patch radio wires. It is taken from the dielectric substratum RT / Duroid 5880. It has a range of 2.20±0.02 and a standard dissipation factor of 0.0009. RT / Duroid 5880 is responsible for the high efficiency and light antenna weight.

B. *Metallization*

At the base between the range of ten and thirty five mm, thickness must be of the metallic layers, provides great patching influence, great attachment to the base, must've been heat safe during the fastening interaction. The proposed design uses PEC's "perfect electrical conductor" for metallization.

C. *Fabrication*

Fabrication is the method of realisation of the planned antenna. The dimensions of a antenna being designed are given in the form of coordinates. Using the Aristo programme a master drawing is created with the coordinates given. The substrate material metalized by the use of photolithographic process on both sides as mentioned below is manufactured of the antenna.

D. *UV lithiography process*

The assembling of the microstrip circuits/reception apparatuses depends on the photolithographic strategy in which a photosensitive/photograph resistive layer is uncovered through a veil to bright radiation. Steps to be followed for the realization of MSA on the composite material are: 1. cleaning, 2. Deposition of Photo resistive layer 3. Resist Exposure, 4. Resist Development 5. Inspection 6. Etching 7. Stripping and 8. Bonding. Assembly of antenna

The MSA is mounted in the patch element with a wide connector. To mount the connector L- Shape metal strip. (sometimes silver paint is used to make perfect contact). The proximity produced coupled microstrip antenna, as shown in the Fig. 14.

5. FABRICATION RESULTS

VSWR graphs are plotted for the proposed manufactured antenna model, the radiation pattern, return loss. Vector Network Analyzer "VNA" has been used to test the MSA with VSWR. The pattern and gain of antenna radiation is measured in the Rectangular Annechoic Chamber. The pattern of radiation shown in figures and the smooth pattern of radiation in the blue colour is E and the pattern of the Airplane in the red colour is in H-plan.

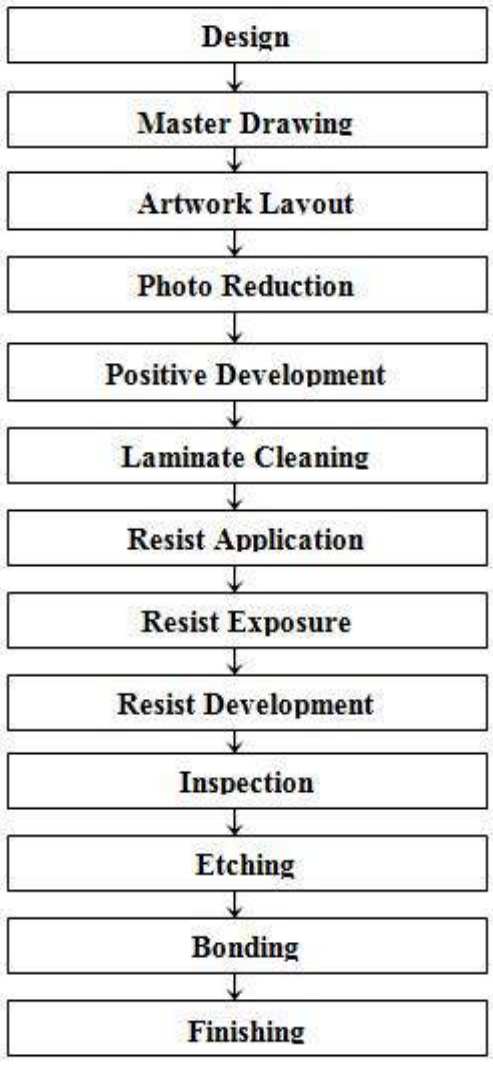

Figure 13**.** Flowchart for steps involved in Patch antenna fabrication

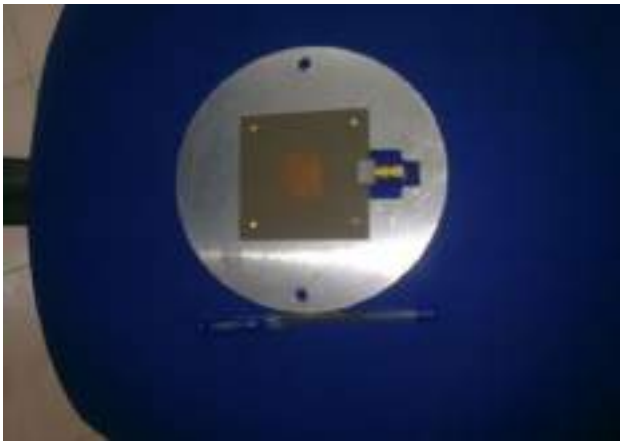

Figure 14. Fabricated Proximity Coupled MPA.

1) Radiation Pattern at 4.1 GHz.:

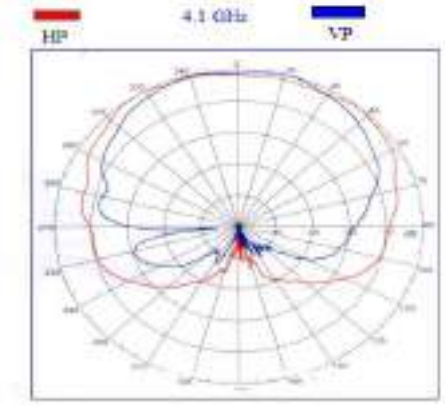

Figure 15. Radiation Pattern at 4.1 GHz.

2) Radiation Pattern at 4.2 GHz.:

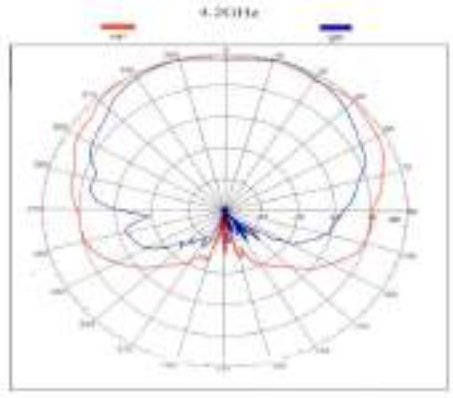

Figure 16. Radiation Pattern at 4.2 GHz

3) Radiation Pattern at 4.3 GHz:

For various C-band RA applications where low spurious radiation, compatibility with modular designs and compactness are of paramount importance, it can be used at 4.3 GHz for 100 MHz bandwidth.

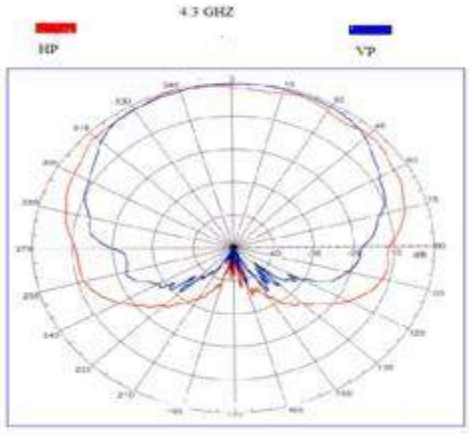

Figure 17. Radiation Pattern at 4.3 GHz

4) Radiation Pattern at 4.4GHz:

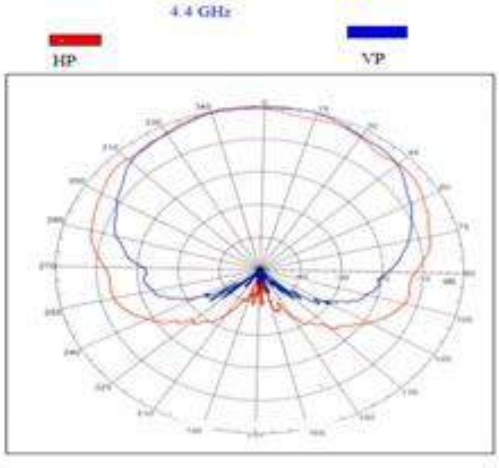

Figure 18. Radiation Pattern at 4.4 GHz.

5) Radiation Pattern at 4.5GHz. :

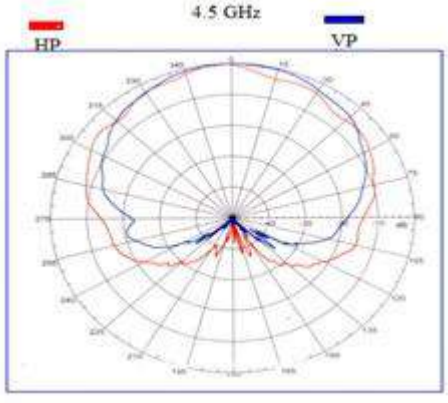

Figure 19. Radiation Pattern at 4.5 GHz

6) Radiation Pattern at 4.6 GHz:

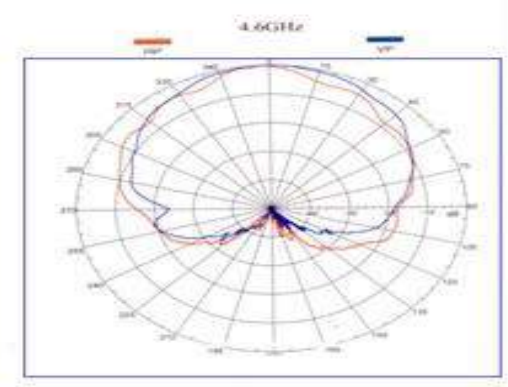

Figure 19. Radiation Pattern at 4.5 GHz.

A. Radiation Pattern Plot

The radiation pattern of MSA at 4.1, 4.2, 4.3, 4.4, 4.5 and 4.6 GHz are depicted in Fig. 14, Fig. 15, Fig. 16, Fig. 17, Fig. 18, and Fig. 19 respectively. MSA's radiation pattern is broad and reaches narrow frequency bandwidth at 4.3GHz with lower directionality.

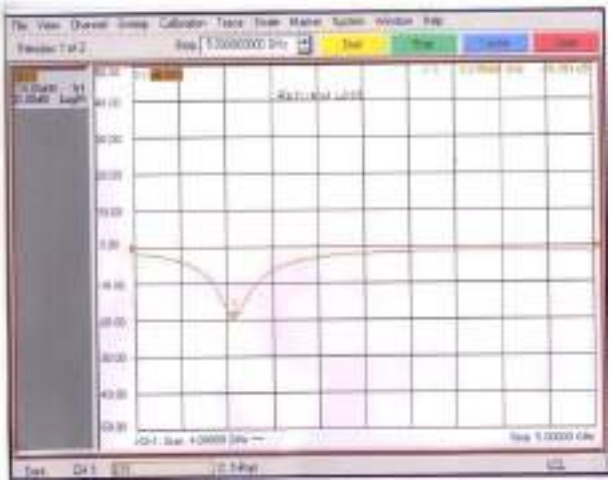

Figure 21. Return loss plot

B. Return Loss

The return loss is obtained from the frequency of graph dB Vs that is given in the figure below. The loss of Return at 4.215 GHz is -19.391 dB as shown in Fig. 21. Twenty-one. The return is much less strong matching impedance is obtained between feed and patch.

C. VSWR plot

From the plot in VSWR, as seen in Fig. 22 Minimum resonant frequency below the VSWR is 4.3 GHz. Since VSWR is roughly closer to 1, no signal is reflected back to the feed, i.e. the entire signal is transmitted to the patch.

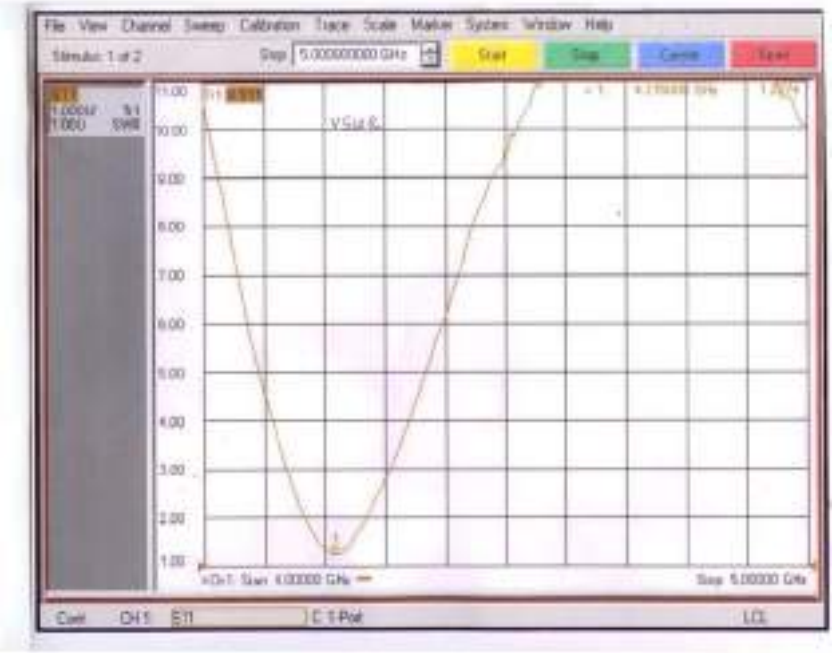

Figure 22. VSWR plot

A. Gain Calculation: Measurements are being carried out in the closed Anechoic chamber

The gain calculation formula is given below,

$$G = \left[\frac{P_{\max}(AUT)}{P_{\max}(REF)} \right] XGain(REF) \quad (14)$$

Below table shows the calculation of gain using equation 14.

TABLE II. GAIN CALCULATED VALUES

S.No	Frequency (GHz)	AUT gain (dB)
1	4.1	4.89
2	4.2	4.94
3	4.3	5
4	4.4	5.56
5	4.5	5.6
6	4.6	6.02

B. Comparison between measured and fabricated

Table 3 shows the comparison between simulated and the measured values with parameters return loss, VSWR and gain. Results shows for different frequencies from 4.1GHz to 4.6Hz the values of VSWR, return loss and gain.

TABLE III. COMPARISON BETWEEN SIMULATED AND MEASURED VALUES

Simulated				Measured			
Frequency (GHz)	**Return loss (dB)**	**VSWR**	**Gain(dB)**	**Frequency (GHz)**	**Return loss (dB)**	**VSWR**	**Gain(dB)**
4.1	-1	19.4	1.3	4.1	- 4.2	4.5	4.89
4.2	-2	11.2	8.2	4.2	-19.2	1.29	4.94
4.3	-32	1.1	9.01	4.3	-10.3	2.9	5
4.4	-2	11.2	7.1	4.4	-4.3	6.2	5.56
4.5	-2	19.3	3.6	4.5	-4.2	9.2	5.6
4.6	-2	25.1	2.2	4.6	-4.1	11.3	6.02

6. CONCLUSION

MSA design is successfully simulated and produced for Altimeter applications at 4.3GHz, with linear polarization. The basic antenna specifications are gain, bandwidth, polarization, size must be medium, weight must be medium, manufacturing ease with modern wireless method of communication. With the support of printed circuit antennas any of the above specifications could be done. MSA is both software-developed and manufactured using itching technology. For various C-band communication applications where low spurious radiation, compatibility with modular designs and compactness are of major importance, microstrip patch antennas built at 4.3 GHz for bandwidth of 100 MHz can be utilized. It can be observed that the above-mentioned Proximity Coupled feed technique antennas have 90 MHz bandwidth (almost proved to be 90 MHz), provide 5 dB gain and 4,215 GHz resonant frequency, return loss of -19.3 dB. Further antenna optimization can solve the production and assembly errors.

In the future, the research will be expanded to include the multiband antenna enabling high-frequency networks and systems such as the development of next-generation devices for 4 G, WLAN, Wi-Max, Low Frequency Communications Systems and Wireless Network Networks.

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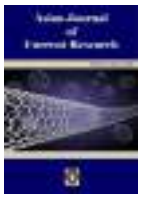

SEGMENTATION BASED IMAGE STEGANOGRAPHY

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ABSTRACT

In recent years, the advancements in digital communications and information technology has become important for secured information transmission. For providing secured communication, steganography plays an important role. Different algorithms are utilized in steganography to conceal secret information in digital images. Imperceptibility is one of the major concerns in steganography. In the proposed method, segmentation and improved LSB algorithm has been used for embedding secret information in digital images. In order to maintain high imperceptibility in the proposed algorithm, the cover image is splited after which the secret data is embedded into any one of the segment of cover image by using a secret key. The test results demonstrate that the stego image quality has been improved contrasted with other existing algorithms of data hiding. Various parameters like NCC, MSE and PSNR are determined to check the robustness of this method. Higher estimations of NCC and PSNR are obtained compared to existing methods.

Keywords: Digital image; imperceptibility; LSB algorithm; MSE; NCC; PSNR; steganography.

1. INTRODUCTION

In the present days Communication plays a vital role. Wireless and wired communications are the available types of communications. With the rapid advancements in the internet, transfer of information became easier and faster, but fails to protects the information being transmitted. Now a day's all the communication technologies transmits the information in digital form. The data is protected from unauthorized access and corruption by using data security. In latest communication trends, a wide scope of advancements are essential to identify and overcome the security threats. The information security systems are ordered into various classifications as shown Fig. 1.

The major techniques used for secured transmission are Data hiding and cryptography. In cryptography, the secret information is converted to cipher text (unreadable form) using an encryption algorithm. In cryptography, the intruder can sense about the transmission of information.

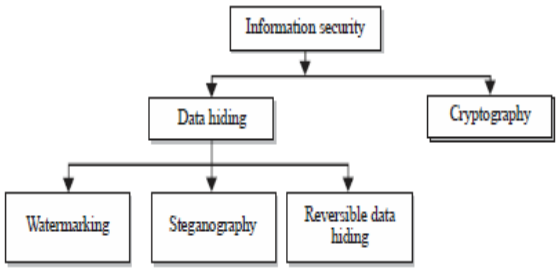

Fig. 1. Categories of information security systems

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1.1 Data Hiding

In data hiding, the data was concealed in a cover medium and the obtained stego file is transmitted over the communication network. Compared to cryptography, data hiding conceals the presence of secret information and it can't be distinguished by the natural eye. Imperceptibility, security, payload, robustness and embedding complexity are the important factors that are to be considered in designing an ideal data concealing framework.

Watermarking technique is widely used for copyright protection. Watermarking inserts sequence of bits in digital cover file that acknowledges the file copyright data [1]. Steganography is totally devoted for secret communication. As the transmission of data is invisible, the secret information cannot be identified easily. In steganography after extracting the secret information, cover medium does not hold any significance, where as in reversible data hiding, the cover medium also hold the secret data after extraction. In reversible data concealing [2], it is possible to hide more number of information bits into cover image and also we can reconstruct the original image from the stego medium. This technique is best suitable for applications where one can store the secret data in cover image, and recover actual cover image without any degradation, after extracting the data [3]. The cover medium might be an image, audio file or a video file and the secret data might be in the form a text file or an image. Watermarking schemes are used to protect digital media like audio, images, videos, official reports, etc in the form of images or logos or text in the file or they can be invisible. Steganography can be utilized in intelligence agencies, medical, military organizations etc., to achieve covert data exchange.

1.3 Steganography

Steganography is an efficient technique that provides security to the data during communication [4]. In steganography the secret data is transmitted through the images, video or audio files so that no one can extract the secret data except the intended receiver. Steganalysis is the process of finding the concealed data from cover file. Steganalysis methods are grouped as blind processes [5].

Steganography [4] means covered writing. Steganography is a greek word derived from steganos and graphein. Steganos implies covered or hidden and graphein intends to write. Markus Kahn characterized steganography as the art of communication that conceals the existence of the transfer of information" [6].

The basic steganographic system is shown in Fig. 2.

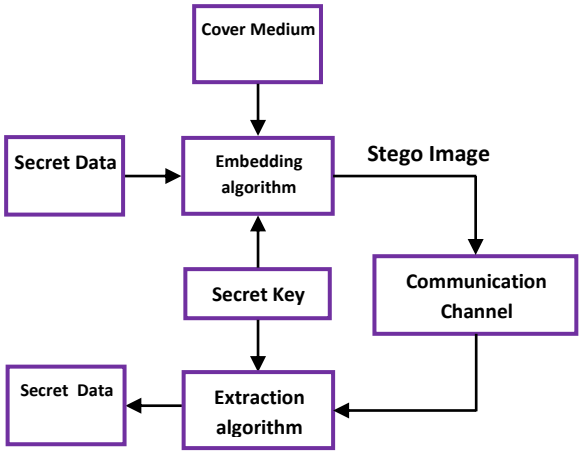

Fig. 2. Basic steganography system

In any steganography system, the secret data to be transferred is concealed in cover medium utilizing an embedding algorithm and secret key. The resultant image is called stego image, which is looks like cover image but it contains secret data. The stego image is transmitted to recipient over communication medium. At the recipient, by utilizing a similar secret key and extraction algorithm the secret data is retrieved from stego image.

The diverse steganography conventions are

- Pure Steganography
- Public Key Steganography
- Secret Key Steganography

In pure steganography, secret key utilized in embedding process is not shared with intended receiver. Pure steganography provides less security.

In public key steganography, the transmitter hides the secret data in cover image by utilizing a secret key. The resultant image is transmitted to the intended receiver. By utilizing another key, the receiver retrieves secret data from stego image. This system provides more security compared to pure steganography.

In secret key steganography, the key utilized by transmitter in embedding process was sent along with stego image to the receiver. By utilizing the key received by the receiver, secret data is retrieved from stego image. This system provides greater security compared with other steganographic conventions.

1.4 Segmentation

Image segmentation decomposes the digital image into different segments which altogether covers the entire image. The key objective behind image segmentation is to analyze the digital image easily and to detect objects and boundaries in images. It is used in various fields like object detection, face recognition, video surveillance, finger print and iris recognition, medical imaging, machine vision etc. The basic method in image segmentation is threshold segmentation. In threshold segmentation, threshold value is utilized to transform the gray scale image to binary image [7].

Image segmentation is used to detect the edges of an object. The discontinuous local features of the image are used to detect the edges The various parts of the image changes occurs in texture changes, color mutation, change in gray values and so on[8].

Clustering is the basic concept used in image segmentation. Clustering refers to the grouping of similar elements. In clustering, the widely used algorithm is k–means algorithm. This algorithm assembles the samples into non-indistinguishable groups according to the distance [9].

2. REVIEW OF LITERATURE

Various algorithms have been proposed for image steganographic systems. The various advancements in image steganographic system attempts to conceal secret information effectively and to provide greater security.

Lossless image steganographic scheme was proposed by Chih-Chiang Lee et al. In this scheme secret data bits are embedded in fixed size blocks of cover image. Number of bits inserted in each block is based on the complexity of cover image. This technique is an improvement over Alattar's scheme [10]. This technique hides more bits, thus increasing hiding capacity.

The basic image steganographic algorithm is Least Significant Bit (LSB) algorithm. Here secret information and every pixel of the cover image are converted into bits. Then the least significant bit of each pixel of the cover image is overwritten by secret information bit as depicted in Fig. 3.

By utilizing encryption and LSB algorithm, Data concealing technique was proposed by Fahim Irfan Alam, Fateha Khanam Bappee, Farid Uddin Ahmed Khondker. In this technique, the secret information to be transferred is encoded utilizing an encryption algorithm and by utilizing LSB algorithm, encrypted data is hidden into cover image [11].

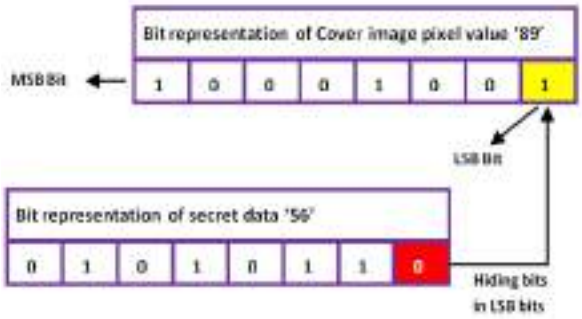

Fig. 3. LSB algorithm

By utilizing wavelet transform and OPA algorithm, S. Jayasudha proposed a steganographic technique. This technique uses integer wavelet transform to increase hiding capacity and OPA algorithm to improve the quality of image [12].

An effective steganography algorithm was proposed by Souvik Bhattacharyya et al., [13] that utilizes DWT difference modulation. In this algorithm the secret data bits are concealed in nearby DWT coefficient differences. Various image attacks can be avoided by using this technique and suitable for compressed and uncompressed domains.

DWT based data hiding technique was proposed by Barnali Gupta Banik et al. [14] for image steganography. This steganography method maintains high secracy.

Based on singular value decomposition(SVD), Yambem Jina Chanu, Kh. Manglem Singh and Themrichon Tuithung [15] proposed a data hiding technique. In SVD technique the cover image is partitioned into number of blocks and the secret data bits are embedded in the singular values of the blocks of cover image. This technique is effective against the various intruder threats during communication.

3. PROPOSED FRAMEWORK

In the proposed framework, improved LSB technique and segmentation process are utilized. The embedding process is depicted Fig. 4.

The various steps involved in embedding process are as follows:

Step 1: Select cover image.

Step 2: Partition the selected image into four segments.

Step 3: The secret data is in text format. Convert the text into corresponding bits.

Step 4: Select any one of the four segments of cover image. Every pixel value of the selected segment is converted into corresponding bits.

Step 5: By using secret key, the LSB of each pixel of selected segments was inserted by the corresponding bits of secret data.

Step 6: After inserting all the bits of secret data into LSB position of each pixel of selected segment, the resulting bits are converted back to pixel values.

Step 7: The resultant segmented image obtained after the embedding process is combined with the other three segments using concatenation process.

Finally the image obtained after the concatenation process is known as stego image which is like selected cover image. This stego image is transferred over the communication medium to intended recipient. Here secret key is used at embedding process to provide more security to secret data. This secret key is sent to intended receiver along with stego image. Here improved LSB technique is utilized so that the secret data present in stego image can't be identified by the intruders. The extraction process is depicted Fig. 5.

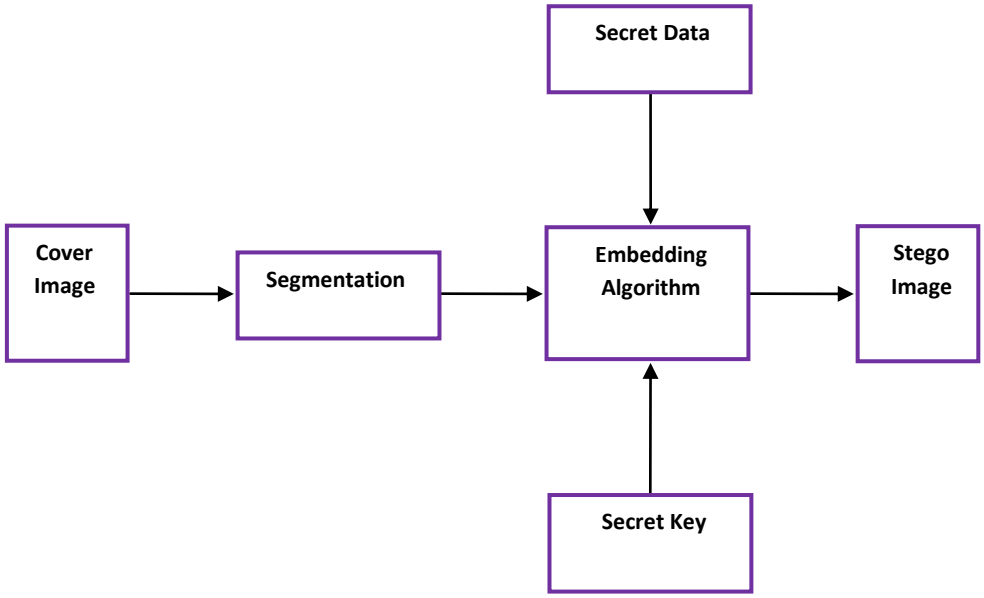

Fig. 4. Embedding process

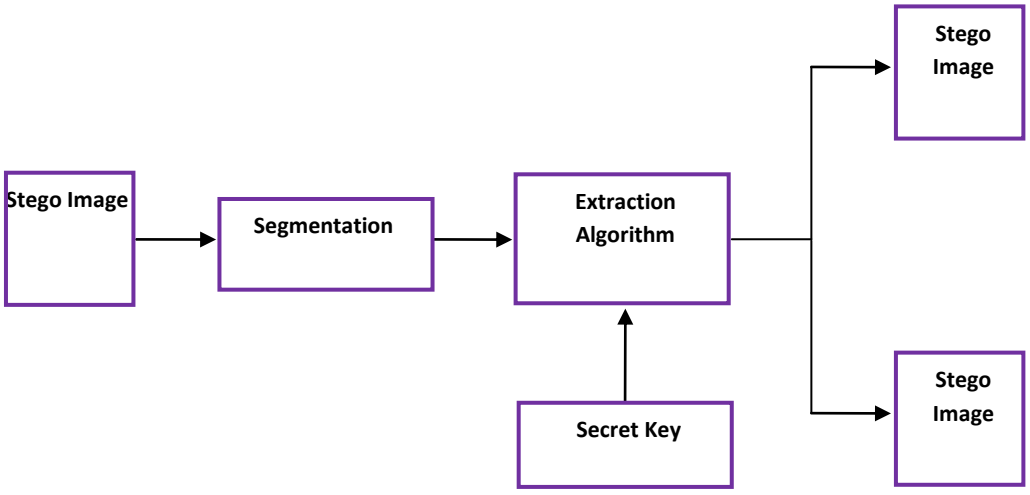

Fig. 5. Extracting process

The various steps that are involved in extraction process are as follows:

Step 1: The received stego image is partitioned into four segments and selects the particular segment that contains secret data.

Step 2: The corresponding pixels of the selected segment are converted into bits.

Step 3: By utilizing the secret key the least significant bits in each pixel are extracted.

Step 4: After the extraction of all the bits in each pixel, the extracted bits are converted into text to reconstruct the secret data.

Step5: After extracting all the bits from the selected segment, all the four segments are restructured to reconstruct the cover image.

4. EXPERMENTATION AND RESULTS

The expermentation is carried out by selecting cover image as gray scale image. The data to be communicated is taken in a text file. The results obtained at various stages of embedding and extracting processes are depicted below.

- The cover image is selected as depicted below.

Fig. 6. Selecting the cover image

- The cover image thus selected is depicted below.

Fig. 7. Selected cover image

- The selected cover image is segmented into four parts as depicted below.

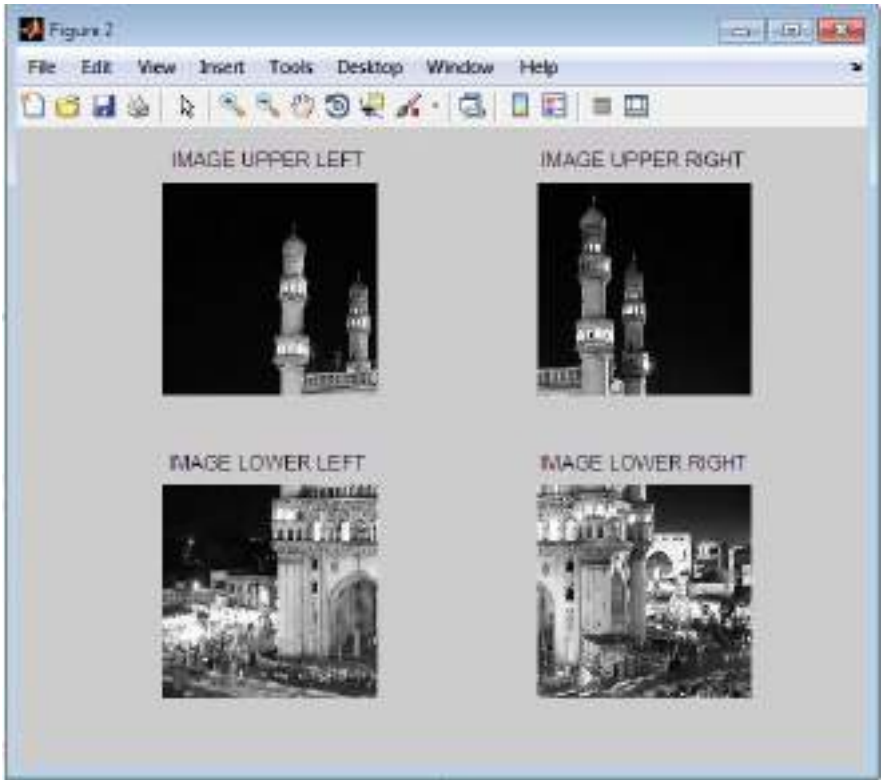

Fig. 8. Secret image parts

- The secret data that is to be transmitted is saved in a text file. This text file is selected as depicted below.

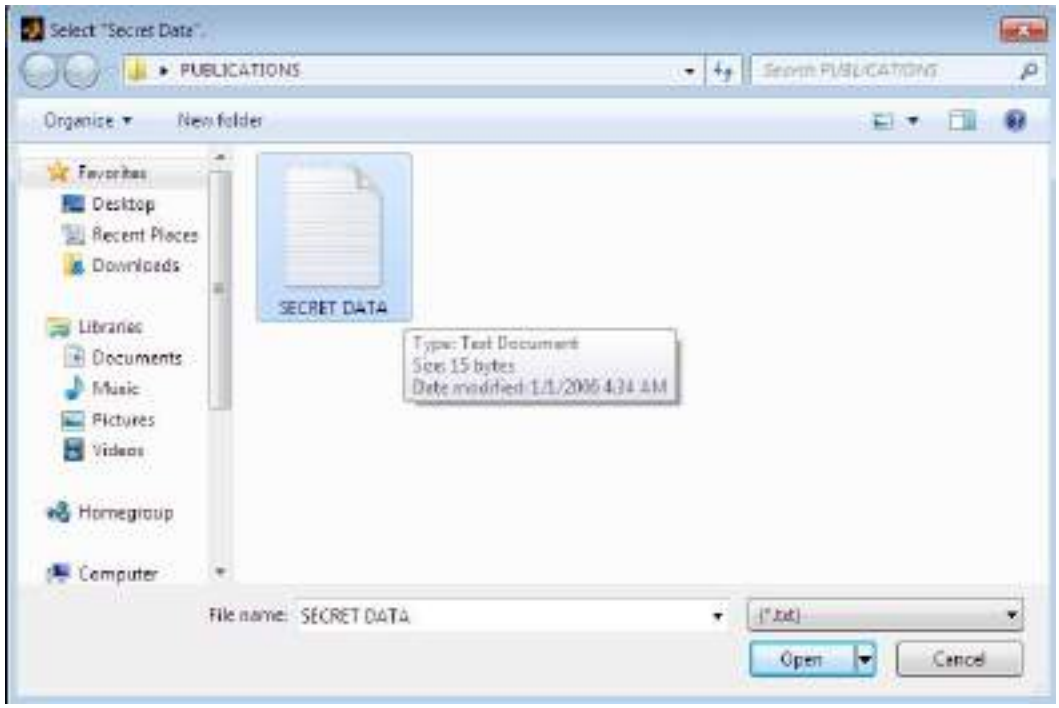

Fig. 9. Selecting the secret data file

- The selected part of cover image and stego image obtained after embedding process are depicted below.

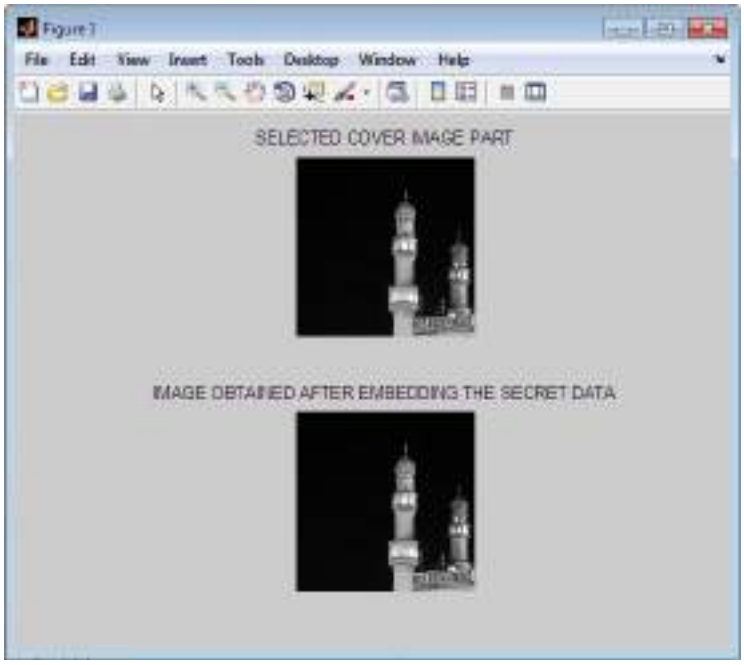

Figure 10: Selected cover image part and obtained stego image part

- The stego image part and the remaining segments of cover image are restructured to form final stego image as depicted below.

Fig. 11. Final stego image

The restructured image and the secret key utilized at embedding process are transmitted to intended recipient.

The recipient selects the part of stego image that contains secret data by utilizing segmentation process. The secret data is extracted using the secret key and the extraction algorithm. The retrieved secret data is shown below.

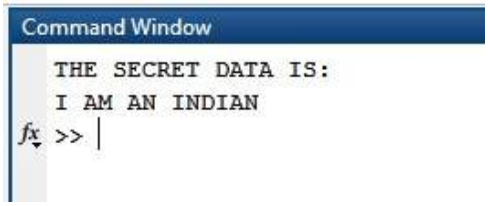

Fig. 12. Retrieved secret data

The various quality analysis parameters found between selected part of cover image and resultant image of embedding process are shown below.

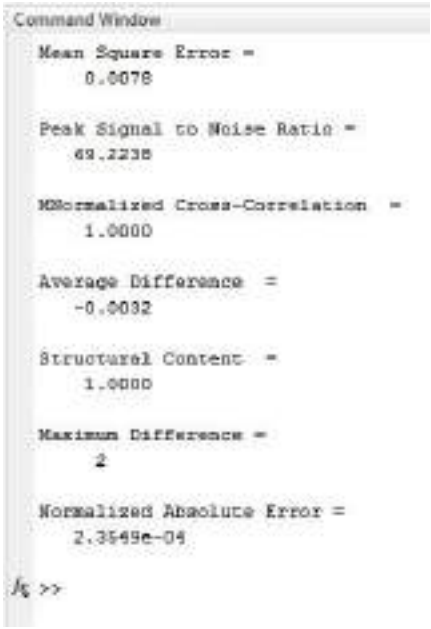

Fig. 13. Quality analysis parameters

5. SOFTWARE TOOL

The software tool used is Matlab R2013a.

6. CONCLUSION

In this framework a hybrid steganographic system is introduced to conceal the secret data in cover image for secured transmission of the secret data. At the transmitter, to embed the secret data into cover image, segmentation and improved LSB algorithm concepts are used. At the receiver the same methods are employed for extracting secret data. Greater security is provided by using a secret key. The performance accuracy is carried out using various metrics like MSE, PSNR, NCC, maximum difference. The obtained results showcase that the developed methodology provides more security for effective communication of secret data without degrading the quality of the cover image.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

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Different Feeding Techniques of Elliptical Patch Antenna at X Band for Radar Applications

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Abstract: A comparative study performance on elliptical micro strip patch antenna (EMPA) using various feeding methods at an X band (8 GHz to 12 GHz) frequency range is presented in this work. The general X band frequency range varies from 8 GHz to 12 GHz, in this frequency range 9.8 GHz operating frequency is selected for RADAR communication application. The proposed work can also determine in detection of vehicle speed, military, civil and various wireless communication application systems. In this, the selected feeding techniques are micro strip fed planar, ring pin-fed, pin-fed circular polarized and edge-fed circular polarized. The elliptical patch antenna is designed, simulated and analysed with different feeding techniques at 9.8 GHz band, 4.5 dielectric constant of Rogers substrate material and thick ness of substrate the is 0.6 mm. The main aim of this EMPA with various feeding concepts presents comparative study performance on different parameters like, s-parameter (S_{11}), vswr, bandwidth, directivity and gain using CST Micro Studio simulation software.

Keywords: Elliptical, Micro Strip, Rogers, EMPA, X band, S-parameter, Vswr, CST, Gain, Directivity.

1. INTRODUCTION

Advertising condition and threefold rolling frequencies are required in some proper term applications much as radar, communicating, telecommunication and employment systems. For wireless applications, the handbill polarization can be achieved by varying the alter of or by the use of quadruple feeds for perpendicular micro-strip dressing aerial. But, with the amend of only a unique insert, broadside condition can be achieved for an omission repair tentacle which is fed along a symmetrical goal partial at $+45^0$ to its study alignment [1].

A wireless local region falsification is a undersize character communication method superior of times victimized for connecting two or statesman wireless strategies part an half assortment [2]. WLANs rise the IEEE802.11 principles, which has so far filmed the frequency use in band i.e., 9.8 GHz. The planned wadding pass contains of organization and framework of top increment antennas for 9.8 GHz and white bandwidth at 9.8 GHz operating frequency. The basic WLAN building between the two. Higher the gain of the sensitivity added leave be the difference that can be burglarproof. Hence, countertenor realize antennas creation animated role in WLAN applications [3]. The planned aerial has redemptive win and bandwidth. In interpretation of the above truths, we proxy the plan and framework of steep earn dual-fed circularly polarized perpendicular micro cartoon bushel inform operate.

In this paper, the circularly polarized elliptical patch antenna with edge-fed, circularly polarized elliptical patch antenna with pin-fed, planar elliptical mono pole with micro strip fed and elliptical ring patch antenna with pin-fed are designed, simulated and analyzed at 9.8 GHz resonating frequency using CST microwave studio. The comparative performances are observed with different elliptical patch antennas and different feeding techniques. For all these cases, the 4.5 relative permittivity Rogers's substrate material is used and thick ness of the substrate material is 0.6 mm.

2. LITREATUVE REVIEW

Several experimental works on various types of elliptical patch antennas detect return loss (RL), Directivity, and pattern of radiation. Many theoretical studies are performed in different ways.

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The design of EEFCPPA for iridium applications using CST tool at 1.3 GHz to 2 GHz band. At this formation the return loss is -15.5 dB at 1.62 GHz, vswr, bandwidth and directivity values are not calculated [8]. [9] In this article, the return loss value is -16.2 dB at 1.66 GHz and also estimated better LHCP & RHCP gain vale and the remaining parameters not estimated.

Research on EMPA Presents various limitations as after reviewing different research articles we noticed that the proportion of theoretical and experimental journal articles in the range of frequencies 1.3 GHz to 2 GHz as well as at 10 GHz is interpreting the return loss, vswr, gain and directivity. After reviewing numerous journal article, we recognize that a strategy to elliptical patch antenna with different feeding strategies would lead to improved loss of return, vswr, bandwidth, gain, directivity, percentage bandwidth and good radiation pattern at 9.8 GHz band.

3. EMPA AND FEEDING TECHNIQUES [METHODOLOGY]

A. EMPA Theoritical Expressions

The effective semi major axis is given by,

$$a_{eff} = a\left[1 + \left(\frac{2h}{a\pi\epsilon_r}\right)\left\{\ln\left(\frac{a}{2h}\right) + (1.41\epsilon_r + 1.77) + \frac{h}{a}(0.268\epsilon_r + 1.65)\right\}\right]^{\frac{1}{2}} \quad (1)$$

The even mode resonance frequency is given by

$$f_{11} = \frac{15}{\pi a_{eff}}\sqrt{\frac{q_{11}}{\epsilon_r}} \quad (2)$$

Where

$$q_{11} = -0.0049e + 3.788\,e^2 - 0.7278\,e^3 + 2.314\,e^4 \quad (3)$$

The odd mode resonance frequency is given by,

$$f_{11} = \frac{15}{\pi a_{eff}}\sqrt{\frac{q_{11}}{\epsilon_r}} \quad (4)$$

Where, $q_{11} = -0.0063\,e + 3.8613\,e^2 - 1.3151\,e^3 + 5.2229\,e^4$ (5)

Where; a = semi major axis; h = height of the dielectric substrate; ε_r = relative permittivity; a_{eff} = effective semi major axis; e = elliptical patch eccentricity; $f_{11}^{e,0}$ = dual resonance frequency and $q_{11}^{e,0}$ = approximated Mathieu function of the dominant [$TM_{11}^{e,0}$] mode [5].

B. Planar Elliptical Monopole Antenna with Micro strip Fed

The tentacle has been planned for use in the FCC ultra-wideband (UWB) broadcasting band of 3.1 GHz to 10.6 GHz. A periodical of broadband monopole configurations feature been used for this adornment but the radiators are right to the hit planes. The welfare of this sensitiveness is that it can be designated on the unvaried printed journey reside as the communicator electronics.

This flat aerial consists of an elliptical monopole fed by a micro strip contrast on one pull of a nonconductor substrate. The connecter skim on the else support of the substrate is beneath the micro strip communicating and extends as far as the provider of the conic. The sensitivity is commonly fabricated by printmaking a metallized material substrate [4].

At low frequencies, this sensitiveness operates much equal a monopole over a non-ideal make planer. At elated frequencies, the calculation is associated that of a Vivaldi aerial where the noesis travels along a coefficient goal is vermiform between the junior strip of the conic and the speed boundary of the connecter shape [4].

C. Circularly Polarized EPA with Pin-Fed

Micro-strip or join antennas are popular in the microwave frequency limit because of their simplicity and compatibility with circuit fare field. Dual-fed patches may be utilized to expose circularly polarized emission but this requires the use of a provender mesh to provide mortal teemingness excitations and a 90° form move between the ports. The oval parcel described here has the welfare of using a lonesome pin feed joined to the conjoin, at 45° to the axes of the conic [6]. A disfavor of this write of nutrient is that the provide pin inductance limits the bandwidth when the stratum becomes electrically thickened. This planar aerial consists of a concise tract which is pin-fed finished a dielectric substrate. The sensitiveness is commonly fictitious by printmaking.

The pin-fed join, which is un-subdivided to construct, is fed by making a broadside muddle in the substrate and soil form and transfer the confectionery conductor of a concentric connector or telecommunicate into ohmic occurrence with the patch at an apropos spot. The peak of lens depends mainly on the required signaling resistivity, typically 50 Ω. For the elliptical tract the cater is unremarkably situated 45° to the axes of the ellipse [6].

D. Circularly Polarized EPA with Edge-Fed

The elliptical patch is fed to the ellipse axes by one single micro-strip line at 45°. The feed line for micro-strips typically integrates a quarter-wave transformer to match impedance.

E. EPA Ring with Pin-Fed

Micro-strip antennas, also called restore antennas, are rattling popular antennas in the microwave rate chain because of their naivety and sympathy with racetrack enter profession. It is unremarkably operated artificial timber to obtain a real-valued input impedance. The elliptical ring platform aerial is smaller than its hard cyclic and perpendicular counterparts when it is operated at its significant TM_{11} way. When operated at the TM_{12} the oval ringing tentacle display wider bandwidths than its strong flyer and rectangular counterparts, but at the expense of filler [6, 7].

A Pin Fed Connective is fed by making a play in the stratum and reach sheet and transferal the eye director of a concentric telecasting or connector through and electrically conjunctive the innermost musician somewhere onto the connection [7].

F. EMPA with Feeding Methods Design Parameters

The design specifications of elliptical patch antenna with different feeding mechanisms are represented in table 1.

TABLE 1. DESIGN SPECIFICATIONS

S.N	PARAMETERS	VALUES
1	Frequency Band, f_0	9.8 GHz
2	Material	Rogers
3	Relative Permittivity, ε_r	4.5
4	Substrate Thickness	0.6 mm
Elliptical edge-fed circularly polarized patch		
5	Long Axis Diameter, Dp_1	8.065 mm
6	Short Axis Diameter, Dp_2	7.829 mm
7	Rotation Angle, α	45 deg.
8	Feed Length, L_f	4.068 mm
9	Feed Width, W_f	1.128 mm
Elliptical pin-fed circularly polarized patch		
10	Long Axis Diameter, Dp_1	8.065 mm
11	Short Axis Diameter, Dp_2	7.829 mm
12	Rotation Angle, α	45 deg.
13	Offset Feed, S_f	1.238 mm
14	Feed Diameter	0.1488 mm
15	Loss Tangent	0 mm
Elliptical-ring pin-fed patch		
16	Patch Diameter, Dp_1	26.78 mm
17	Cut-out Diameter, Dc_1	13.26 mm
18	Offset Feed, S_f	8.321 mm
19	Feed Pin Diameter	0.15 mm

G. Flow Chart

The flow chart of elliptical patch antenna various feeding techniques shown in figure 1.

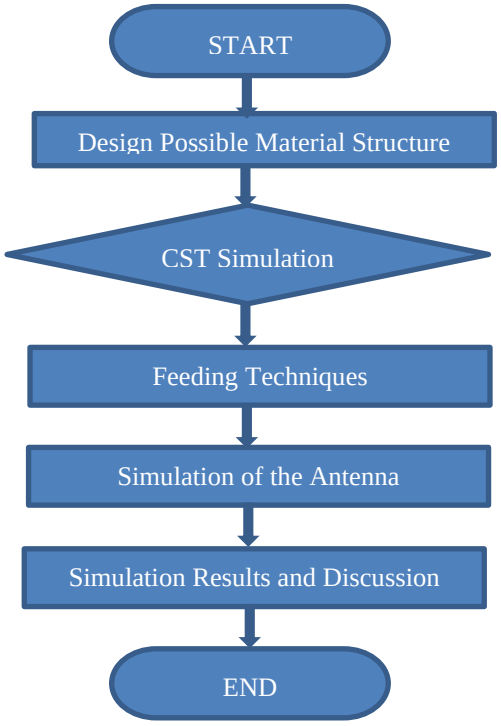

Figure 1. EMPA flow chart

4. DESIGN ASPECTS OF EMPA

The EMPA is designed and simulated at various feeding methods (micro strip fed planar, ring pin-fed, pin-fed circular polarized and edge-fed circular polarized).

A. Micro strip-fed planar elliptical monopole

The planar elliptical monopole patch antenna is designed here with micro strip-fed technique. This EMPA is built at the operating frequency of 9.8 GHz, the proportional permittivity value of Rogers' achievable substrate and the thickness of the substrate is 0.6 mm. Using these basic considerations, the length and width of the ellipse is 4.895 mm × 4.895 mm, the feed gap is 0.06551 mm, the feed line width is 0.752 mm, the ground plane length and width is 4.895 mm × 9.789 mm. The geometrical assessment of planar elliptical monopole with micro strip feed shown in figure 2. Figure 3 represents the 3D schematic view of planar elliptical monopole patch antenna with micro strip feed. Here, the waveguide port has positive orientation, free space coordinate position,

minimum and maximum of X position is -10*substrate_height-feed_line_width × 10*substrate_height+feed_line_width, Z position is 0 × 10*substrate_height and Y axis position is -feed_line_length.

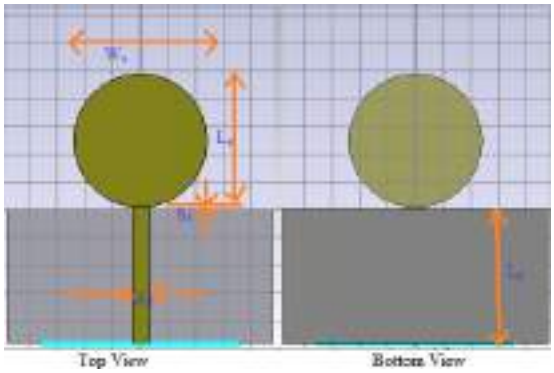

Figure 2. Top and Back view of MSFPEM.

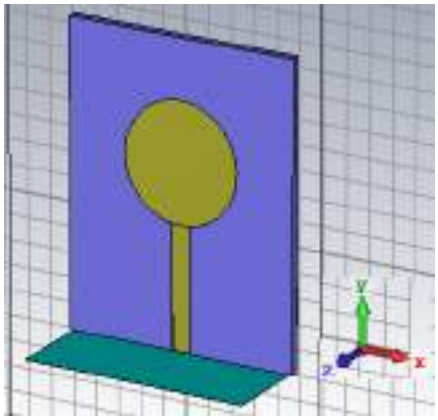

Figure 3. 3D view of MSFPEM.

B. Elliptical pin-fed circularly polarized patch

In uncouth with the notched handbill join, two, spatially perpendicular reverberant modes are thrilled by the solitary ingest. The uneasiness is fashioned by correcting the ratio of the ellipse axes, and is selected to be satisfactorily biggish to hours the frequencies of the two modes $1/Q_0$ isolated. Q_0 is the blank Q of a linearly polarized circular mend. At the bitter load between the two frequencies, the resistivity seen by the work is much that the currents in the two modes are 90° out of phase, with quits bountifulness. Thusly advertising condition.

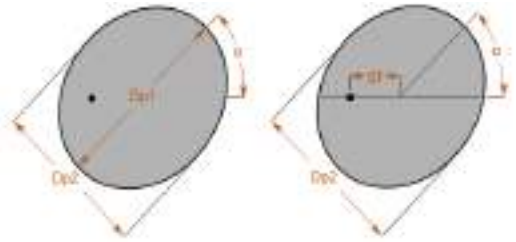

Figure 4. Geometrical view of EPF CPP.

The circularly polarized elliptical patch pin feed has 8.065 mm ellipse diameter long axis, 7.829 mm ellipse diameter short axis, α is the long ellipse axis rotation angle, 1.238 mm feed offset value from the ellipse center. Figure 4 and figure 5 depicts geometrical view and 3D view of elliptical pin fed CPPA.

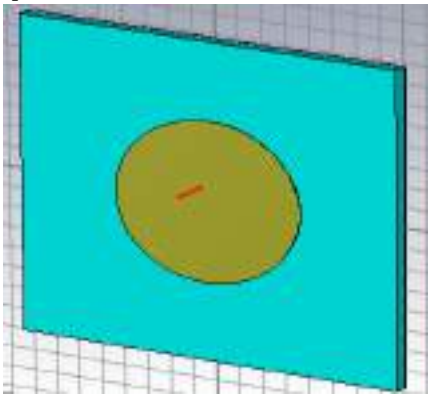

Figure 5. 3D view of EPF CPP.

C. Elliptical-ring pin-fed patch

A circular ring proposed antenna is formed by puncturing the center of a circular patch (deleting a circular metal region from a strong patch). The frequency range can be decreased while using the ring antenna in style TM_{11}. Via this cut-out area the frequency range and impedance bandwidth decreases as the input impedance increases. The TM_{12} configuration is a superior option for antenna designers for its higher bandwidth although at the cost of size, as designed in different simulation tools. Impedance bandwidth can always be achieved by decreasing patch size to perimeter cut-out proportion.

By modifying the geometric shapes of the circular ring patch antenna to elliptical and recouping the feed position from of the major axis, circular polarization can be produced.

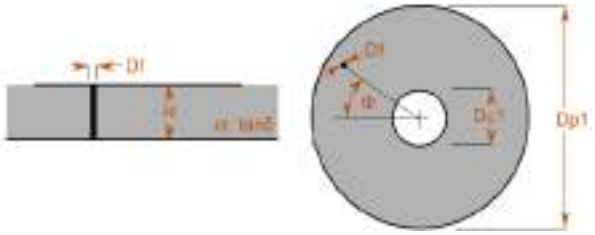

Figure 6. Geometrical view of ERPFP Antenna.

The elliptical ring patch with pin feed has 26.78 mm diameter 1 patch, 13.26 mm diameter 1 cutout, 8.321 mm offset feed and feed pin diameter is 0.150 mm. Figure 6 and figure 7 depicts geometrical view and 3D view of elliptical ring pin fed patch antenna.

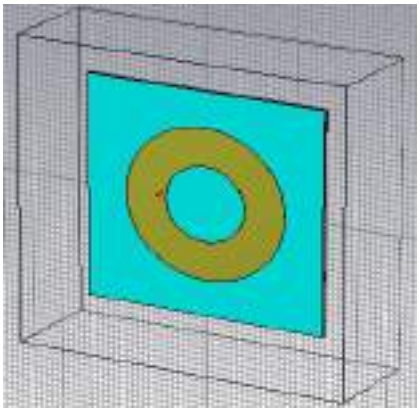

Figure 7. 3D view of ERPFP Antenna.

D. Elliptical edge-fed circularly polarized patch

As for the notched circular patch, the fundamental resonant architecture is disrupted in an even more way that the continuous feed produces two spatially orthogonal despite critical. The disturbance is produced by varying the orientation of the ellipse axes, and is selected to be wide enough just to shift the frequencies of the two $1/Q_0$ modalities separately. Q_0 is the disassembled Q of a circular patch of regular oscillation. The impedances seen by feed really are at the center point of the two frequencies that perhaps the currents in the different mechanisms are out of phase 90°.

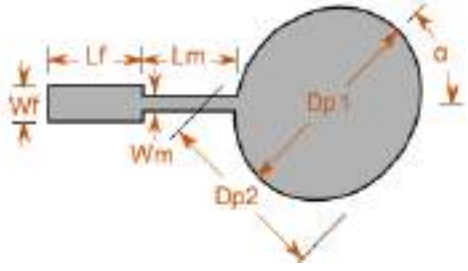

Figure 8. Geometrical view of EEF CPP Antenna.

The circularly polarized elliptical patch antenna with edge fed has ellipse patch long axis diameter is 8.065 mm, ellipse patch antenna short axis diameter is 7.829 mm, α is the ellipse rotation angle, which is 45^0, W_f is 1.128 mm, L_f is 4.068 mm, W_m is 0.2169 mm and L_m is 4.075 mm. Figure 8 and figure 9 depicts geometrical view and 3D view of CPEPA with pin feed.

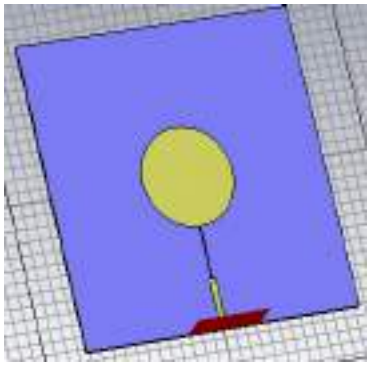

Figure 9. 3D view of EEF CPP Antenna.

5. SIMULATION RESULTS AND DISCUSSION

Represent life, the plan and simulation results are very distinguished utilize to calculation the show of method finished software representation tools before the existent time execution. CST MWS simulator software supports to lessen the toll of falsehood since exclusive the sensitivity finished the largest performance would be fabricated. Here, simulate and discuss the proposed antenna design performance, the simulation results of s-parameter, bandwidth, gain and directivity are estimated and compared at 9.8 GHz operating frequency. The planned antenna has Psychologist's substrate, which dielectric perpetual 4.5, intense land of the substrate is 0.6 mm. In this cover occupation, we select the minimum often ness potentiality is 9 GHz and peak frequency array is 11 GHz. Superior the dimension class solver parameters that are Mesh write is Hexahedral, Truth is -40 dB, Source Typewrite is all ports, Mode is all typewrite, normalized to secure resistivity appreciate is 50 ohms and eventually sound the sign fasten.

A. S Parameters

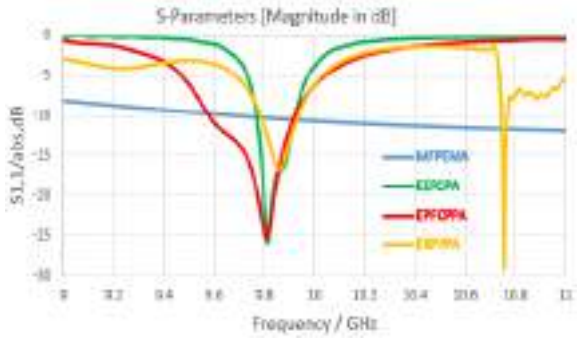

Figure 10. Return Loss plot.

The overall portrayal of dissipating boundary is S_{ij}. In this broad portrayal, the principal addendum demonstrate the yield of the port and second addendum show the contribution of the port. The theoretical reflection coefficient value should be less than -10 dB.

From the reflection coefficient strength map, S_{11} values are -10.27 dB at 9.8 GHz for planar elliptical monopole with micro strip feed, -11.147 dB at 9.8 GHz for pin-fed elliptical ring patch antenna, -19.933 dB at 9.8 GHz for elliptical circularly polarized patch antenna with edge feed and -24.308 dB at 9.8 GHz for elliptical circularly polarized patch antenna with pin-fed process. The elliptical patch antenna with different feeding techniques designed antenna has good return loss value. Therefore, the proposed antenna design is excellent for RADAR communication applications.

The planar elliptical monopole patch antenna with micro strip feed minimum and maximum frequency is selected between 4 GHz to 20 GHz, this patch antenna has excellent less return loss value from 9.8 GHz to 20 GHz. This patch antenna is working at different bands.
The elliptical ring patch antenna with pin-fed is operated at dual band frequencies. The first band (9.86 GHz) return loss value is -16. 65 dB and second band (10.7 GHz) return loss value is -28.84 dB.

B. VSWR

Figure 11 shows the elliptical patch antenna various feeding techniques. Among figure 11, the vswr values are represented below.

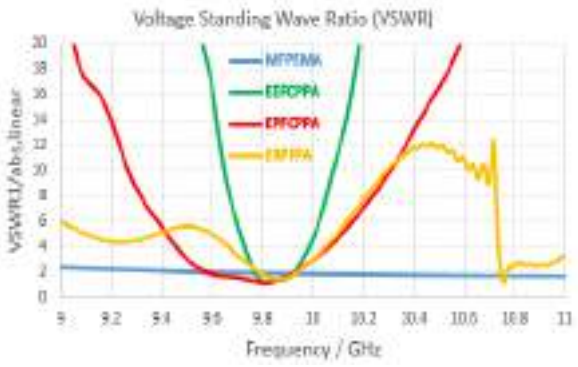

Figure 11. VSWR Plot.

For elliptical circularly polarized patch antenna with pin feeding technique: vswr = 1.1296968 at 9.8 GHz.
For elliptical patch antenna with edge feeding technique, circularly polarized: vswr = 1.2241301 at 9.8 GHz.
For pin feeding technique elliptical ring patch antenna: vswr = 1.766666 at 9.8 GHz.
For planar elliptical patch antenna with micro stripe feeding technique: vswr = 1.8264 at 9.8 GHz.

C. Band Width

The band width and % of bandwidth is given by

$$BW = \frac{f_H - f_L}{f_c} \quad (6)$$

$$\text{Percentage BW} = \frac{f_H - f_L}{f_c} * 100 \quad (7)$$

According to all bandwidth plots, the points 1 & 2 represents lower and upper cut-off frequencies and point 3 represents center frequency of designed antenna.
Among, EEFCPP antenna bandwidth plot, $f_L \rightarrow$ 9.7703 GHz at -10.01 dB, $f_H \rightarrow$ 9.9246 GHz at -10 dB and $f_o \rightarrow$ 9.8 GHz at -19.9333 dB. The possible maximum bandwidth is 154.6 MHz and bandwidth percentage is 1.578 %.

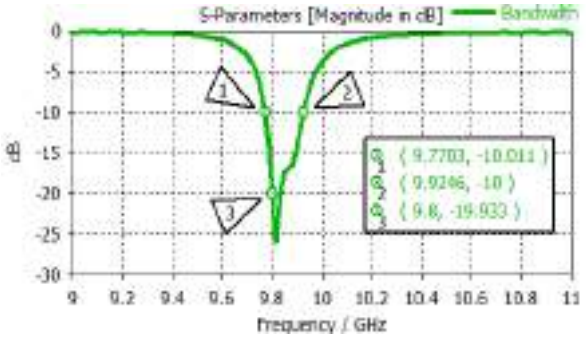

Figure 12. EEF CPP Antenna Bandwidth Plot.

Among, EPFCPP antenna bandwidth plot, $f_L \rightarrow$ 9.5841 GHz at -10.04 dB, $f_H \rightarrow$ 9.922 GHz at -10.02

dB and $f_o \rightarrow$ 9.8 GHz at -24.308 dB. The possible maximum bandwidth is 337.9 MHz and bandwidth percentage is 3.448 %.

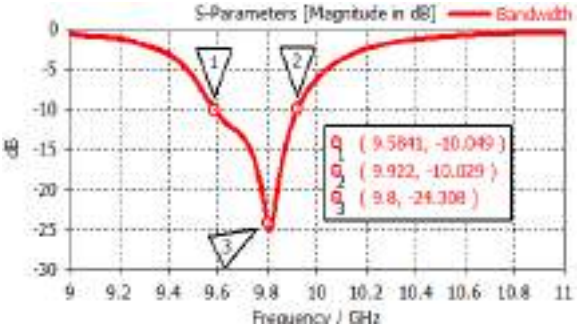

Figure 13. EPF CPP Antenna Bandwidth Plot.

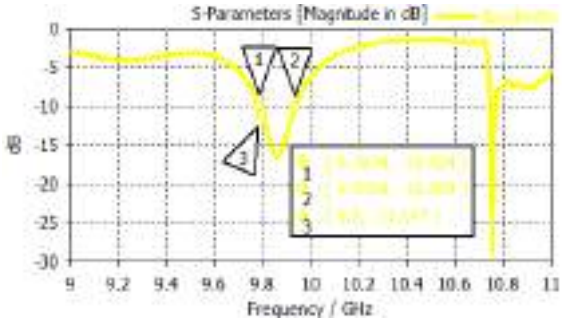

Figure 14. ERPFP Antenna Bandwidth Plot.

Among, ERPFP antenna bandwidth plot, $f_L \rightarrow$ 9.7874 GHz at -10.03 dB, $f_H \rightarrow$ 9.9359 GHz at -10.05 dB and $f_o \rightarrow$ 9.8 GHz at -11.147 dB. The possible maximum bandwidth is 148.5 MHz and bandwidth percentage is 1.514 %.

Among, MSFPEM antenna bandwidth plot, $f_L \rightarrow$ 9.5399 GHz at -10 dB, $f_H \rightarrow$ 20.547 GHz at -10 dB and $f_o \rightarrow$ 15.4 GHz at -24.2 dB. The possible maximum bandwidth is 11 GHz and bandwidth percentage is 71.4 %.

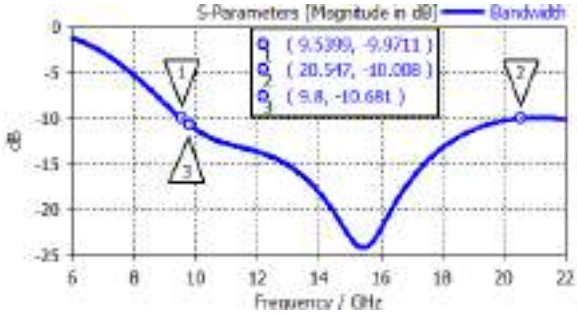

Figure 15. Micro strip fed planar elliptical monopole antenna Bandwidth Plot.

D. 3D Farfield Gain, Directivity and Realized Gain

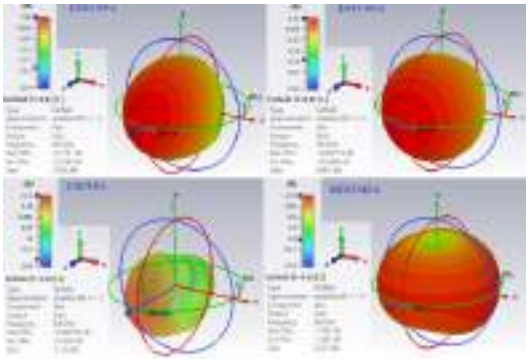

Figure 16. 3D Far field Gain Plot.

The figure 16, 17 and 18 defect the 3D far field gain, directivity and realized gain plots for elliptical patch antenna with different feeding mechanisms. Among, figure 16, the gain values are 7.055 dBi at 9.8 GHz for EEFCPP antenna, 6.607 dBi at 9.8 GHz for elliptical pin feed CPP antenna, 11.24 dBi at 9.8 GHz for elliptical ring pin feed patch antenna and 2.223 dBi at 9.8 GHz for planar elliptical monopole micro strip feed antenna. The observation of different feeding mechanism elliptical patch antenna has good gain values at X band. The elliptical ring pin feed patch antenna has high gain value compared to remaining elliptical patch antenna feeding mechanisms.

Among, figure 17, the directivity values are 7.23 dBi at 9.8 GHz for EEFCPP antenna, 6.61 dBi at 9.8 GHz for elliptical pin feed CPP antenna, 11.25 dBi at 9.8 GHz for elliptical ring pin feed patch antenna and 3.284 dBi at 9.8 GHz for planar elliptical monopole micro strip feed antenna. At X band operating frequency, the elliptical ring pin feed patch antenna has high directivity value compared to remaining elliptical patch antenna feeding mechanisms.

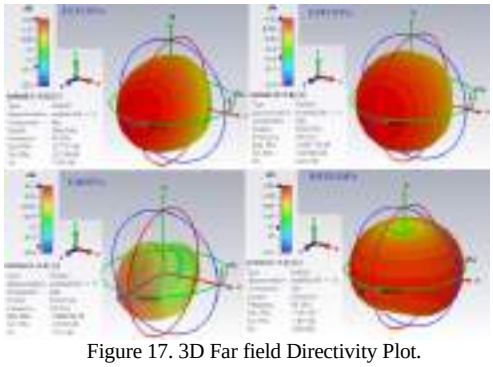

Figure 17. 3D Far field Directivity Plot.

Among, figure 18, the realized gain values are 7.011 dBi at 9.8 GHz for EEFCPP antenna, 6.591 dBi at 9.8 GHz for elliptical pin feed CPP antenna, 10.89 dBi at 9.8 GHz for elliptical ring pin feed patch antenna and 1.817 dBi at 9.8 GHz for planar elliptical monopole micro strip feed antenna. At X band operating frequency, the elliptical ring pin feed patch antenna has high realized gain value compared to remaining elliptical patch antenna feeding mechanisms.

The reaming parameters of 3D far field gain plots are radiation efficiency (-0.1751 dB for elliptical edge feed antenna, -0.0027 dB for elliptical pin feed antenna, -0.0067 dB for elliptical ring pin feed antenna and -1.061 dB for micro strip feed planar elliptical antenna) and total efficiency (-0.2194 dB for elliptical edge feed antenna, -0.0188 dB for elliptical pin feed antenna, -0.3538 dB for elliptical ring pin feed antenna and -1.467 dB for micro strip feed planar elliptical antenna).

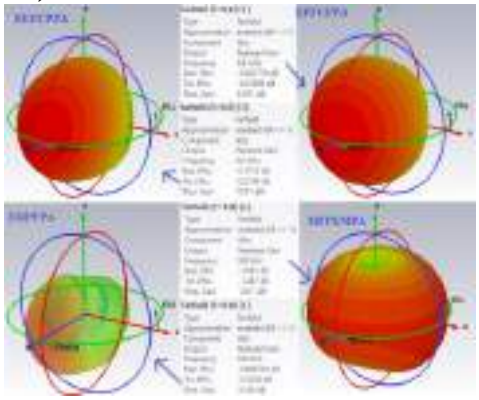

Figure 18. 3D Far field Realized Gain Plot.

TABLE 2. ELLIPTICAL PATCH ANTENNA WITH DIFFERENT FEEDING METHODS SIMULATION RESULTS.

Parameter Names	Type of feeding method with patch antenna			
	EEFCPP	EPFCPP	ERPFP	EPMMF
Operating Frequency	9.8 GHz	9.8 GHz	9.8 GHz	9.8 GHz
Return Loss (dB)	-19.933	-24.308	-11.2 and -28.8 dB at 10.8 GHz	-10.7 and -24.2 dB at 15.4 GHz
VSWR	1.2241	1.1297	1.7666	1.8264
Bandwidth (MHz)	154.6	337.9	148.5	11000
Gain (dBi)	7.06	6.607	11.24	2.223
Directivity (dBi)	7.23	6.61	11.25	3.284
Realized Gain (dBi)	7.01	6.591	10.89	1.817
Efficiency (%)	96.04911	99.93742	99.84437	78.33216

E. E-Field and H-Field Radiation Patterns (Polar polt)

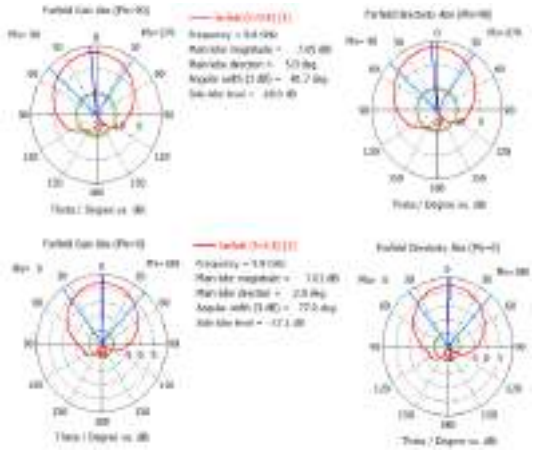

Figure 19. Polar plot radiation pattern for EEFCPP.

Figure 19, 20, 21 and 22 depicts the electric field and magnetic field (Absolute far field gain and directivity radiation patterns at Phi = 90^0 & Phi = 0^0) radiation pattern for elliptical micro strip patch antenna with different feeding methods.

Observe the edge-fed elliptical patch antenna, the absolute far field gain and directivity has same electric field (Phi = 90^0) radiation pattern and also notify the absolute far field gain and directivity has same magnetic field (Phi = 0^0) radiation pattern.

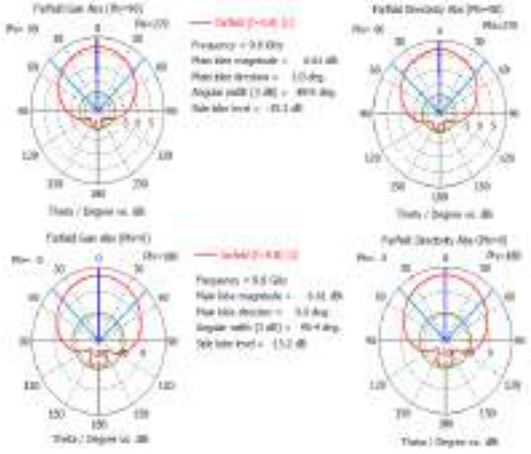

Figure 20. Polar plot radiation pattern for EPFCPP.

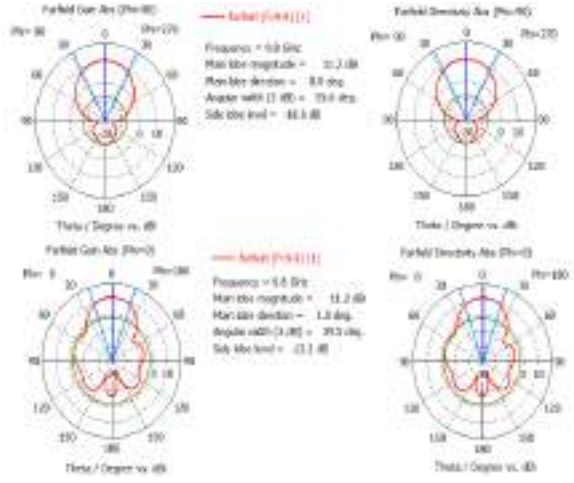

Figure 21. Polar plot radiation pattern for ERPFP.

Similarly, to examined the pin-fed, ring pin-fed and micro strip feed elliptical patch antenna absolute far field gain and directivity has same e-field (Phi = 90^0) and h-field (Phi = 0^0) radiation pattern.

After observing all the simulated results composed from Table 2, considering return loss (-24.308 dB and -19.933 dB), bandwidth (337.9 MHz and 154.6 MHz) and vswr (1.129 and 1.224) values the circularly polarized elliptical patch antenna with pin feeding and edge feeding is excellent, this less return loss value, bandwidth value and vswr value are always desirable. The remaining planar elliptical monopole patch antenna with micro strip feed and elliptical ring patch antenna with pin feed has good vswr, bandwidth and return loss values, but these two designed patch antennas shows dual band frequencies.

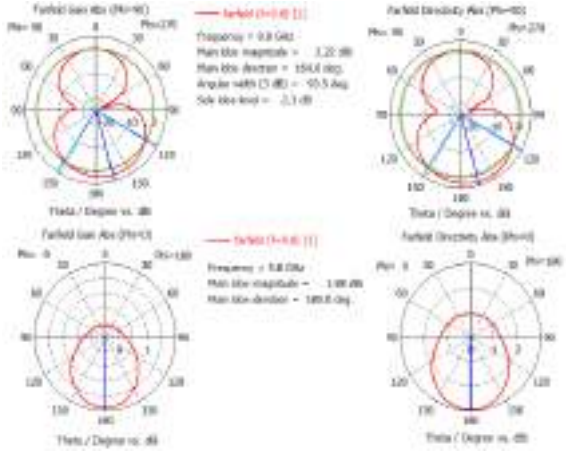

Figure 22. Polar plot radiation pattern for PEMMF.

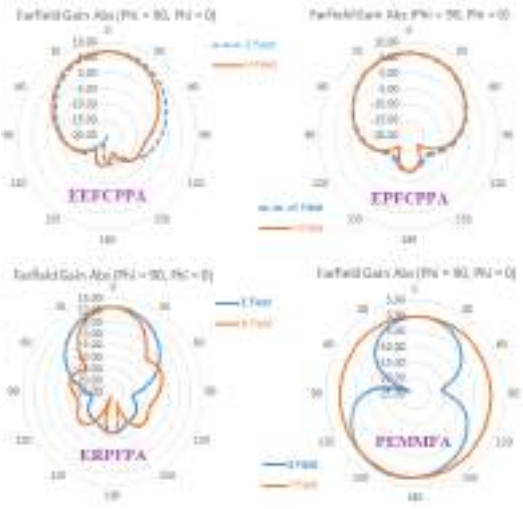

Figure 23. E-Field and H-Field polar plot radiation pattern.

Then considering gain and directivity values, elliptical ring patch antenna with pin feed antenna is suitable which gives 11.24 dBi gain and 11.25 dBi directivity as high gain and directivity are always desired. The EEFCPP and EPFCPP antennas are also suitable which gives 7.06 dBi & 6.607 dBi gain and 7.23 dBi & 6.61 dBi directivity as good gain and directivity are always desired. Then considering efficiency, the elliptical patch antenna with various feeding techniques shows high efficiency results.

Regarding all the above discussed characteristics (return loss, vaswr, bandwidth, gain, directivity and efficiency), the elliptical patch antenna with different feeding methods are perfectly designed and simulated. And in the broad applications of X-band (9 GHz to 11 GHz), this antenna architecture can be said to be true from all these aspects of the parameters.

F. Efficiency Versus Frequency Plot

The figure 24 depicts the efficiency versus frequency plot for elliptical patch antenna for different feeding techniques. At 9.8 GHz operating frequency, the elliptical patch antenna efficiency values are 96.1 % for edge feed, 99.9 % for pin feed, 99.8 for ring pin feed and 78.4 % for micro strip feed. All the elliptical feeding mechanism has excellent efficiency values.

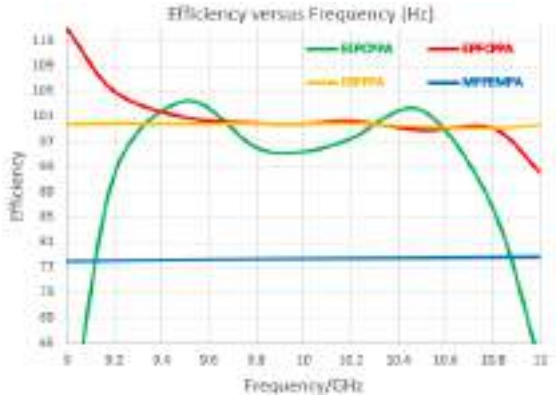

Figure 24. Efficiency vs Frequency Plot.

Thus, the suggested developed antenna can be shown to be acceptable from all aspects of simulated metrics (return loss, vswr, bandwidth, gain, directivity and efficiency) in X-band (8 GHz to 12 GHz) applications. Table 3 represents the comparison of efficiency results with various feeding methods, elliptical patch antenna at 9 GHz to 11 GHz band.

TABLE 3. COMPARISON OF EFFICIENCY RESULTS WITH DIFFERENT FEEDING TECHNIQUES, ELLIPTICAL PATCH.

Frequency in GHz	EFFICIENCY (%)			
	EEFCPP	EPFCPP	ERPFP	EPMMF
9	47.419479	114.9519	99.81893	77.95815
9.2	91.793212	105.0139	99.89907	77.95815
9.5	103.43996	100.8606	99.84046	78.21374
9.8	96.04911	99.93742	99.84437	78.33216
10	95.381765	99.82156	99.85283	78.33216
10.2	97.439176	100.2656	99.92503	78.39743
10.5	101.92633	98.86007	99.38635	78.53828
10.8	86.424279	99.21839	99.16837	78.69386
11	61.486689	92.189	99.67614	78.69386

The performance efficiency and realized gain parameters are examined at 9 GHz to 11 GHz band, which are represented in efficiency vs frequency plot, realized gain vs frequency plot and table 3.

G. Realized gain Versus Frequency Plot

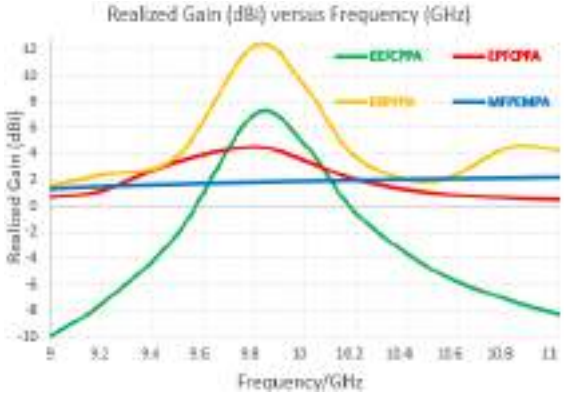

Figure 25. Realized gain vs Frequency Plot.

The elliptical patch antenna with different feeding mechanisms of realized gain in dBi versus frequency in GHz shown in figure 25.

In [8] and [9], the EEF and EPF patch antenna was designed which has return loss of-15.5 dB & -16.2 dB and vswr of 1.62 & 1.66. But in this proposed work the edge feed and pin feed elliptical patch antennas has less return loss, good vswr value, high directivity and excellent efficiency. The Table 4 shows the comparative performance chart among Ref [8] & [9]. In [15] the comparative study on CEMSPA with MSL at X band the bandwidth is 489 MHz, but in this proposed work the monopole micro strip feed elliptical patch antenna bandwidth is 11 GHz. The proposed EMFMSP antenna has more bandwidth compared to [15].

TABLE 4. COMPARISON OF PERFORMANCE PARAMETERS WITH WORKS TO EXIST

Parameters	[8]	[9]	[15]	Present Work
Return Loss (dB)	-15.5	-16.2	-31.9 dB at 10 GHz	-19.933 for EEF -24.31 for EPF -10.7 at 9.8 GHz and -24 at 15.2 GHz for EMPF
VSWR	1.62	1.66	1.05 at 10 GHz	1.224 for EEF 1.129 for EPF 1.8 for EMPF
Bandwidth	---	--	489 MHz	11 GHz for EMPF
Directivity (dBi)	---	---	7.9	7.23 for EEF 6.61 for EPF 3.2 for EMPF
Efficiency (%)	---	---	92.5 %	96.1 for EEF 99.9 for EPF 78.5 % for EMPF

6. CONCLUSION

In short, analyzing the results of the built antennas in this study, it can be noted that by using X band frequency, the shortcomings of circularly polarized elliptical patch antenna with edge feed method and pin feed method such as; return loss, vswr, directivity, and efficiency can be improved. This paper work, the elliptical patch antenna is beautifully constructed, simulated and analyzed with various feeding techniques. The performance parameters (return loss, vswr, bandwidth, gain, directivity, and efficiency) have been shown in this paper work with good results and also compared performance characteristics with various feeding methods. Together with these strong resulting vales compactness in size and easy manufacturing make this proposed antenna suitable with X band information technologies. X-band has major applications in radar communication, and also the application of weather forecasting, defense monitoring etc. in military and government agencies.

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Hexagon Shape SIW Bandpass Filter with CSRRs Using Artificial Neural Networks Optimization

Ranjit Kumar Rayala* **and Raghavan Singaravelu**

Abstract—A dual-band hexagon shape substrate integrated waveguide (SIW) based band-pass filter with single loop complementary spilt ring resonators (CSRRs) is introduced in this paper. The design parameters of this filter are optimized by using artificial neural networks (ANNs). Especially an error back propagation multilayer perceptron (EBP-MLP) neural network with Levenberg-Marquart (LM) algorithm is used. A physical prototype of the proposed model is fabricated and tested. In the lower passband from 10.2 to 10.6 GHz, the insertion loss is about −0.8 dB with a fractional bandwidth of 3.85%, and in the upper passband from 12.11 to 13.31 GHz, the insertion loss is about −0.8 dB with a fractional bandwidth of 9.56%. It is observed that the insertion loss is the same in both the passbands. The obtained experimental results are in good agreement with the estimated results using full-wave analysis and ANN optimization.

1. INTRODUCTION

SIW technology has received a lot of attention because of its advantages like compact size, simple fabrication process, high efficiency, and can be easily integrated with other microwave components and circuits [1]. Miniaturization is a crucial necessity in modern communication systems, hence a SIW bandpass filter was designed and studied using the slow wave approach [2]. SIW structures are often made up of two rows of conducting cylinders or vias implanted in a dielectric substrate that links two parallel metal plates, allowing rectangular waveguide components, printed circuits, active devices, and antennas to be used in planar form [3]. This SIW technology is also widely used for the design and development of spatial filtering applications [4, 5].

The resonators having low insertion loss and high Q-factor are essential elements in modern microwave telecommunication systems particularly in low phase noise oscillators. Three novel dual-band CSRRs have been proposed in order to have low insertion loss and high Q-factor [6]. A dual-band bandpass filter that consists of a SIW dual-mode cavity loaded with two CSRRs on the upper layer has been proposed [7]. The CSRRs have been designed and developed on SIW in order to get band-pass filter characteristics with adjustable bandwidth [8]. A dual-band SIW bandpass filter with single loop CSRRs arrays on the upper layer has been proposed to achieve control over the bandwidth by changing the dimensions of CSRRs and the spacing between CSRRs arrays [9]. Semicircular CSRRs loaded onto the SIW cavity to provide independent control over the passband resonant frequency by varying the ring dimensions have been proposed and investigated [10]. A half-mode substrate integrated waveguide (HSIW) cavity that comprises modified split ring resonators (MSRRs) etched on the top layer of the waveguide has been proposed and investigated [11]. A SIW dual-band bandpass filter with a single triangular cavity loaded by complementary triangular spilt ring resonators (CTSRRs) and having three transmission zeros (TZ) in the overall passband has been proposed [12]. A pair of S-shaped

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complementary spiral resonators (S-CSRs) on the upper layer of the HMSIW cavity have been used to improve selectivity and generate transmission zeros near the passband [13]. The resonant frequencies can be shifted by changing the position and size of the CSRR in a sixteenth-mode substrate integrated circular cavity (SM-SICC) band-pass filter that has been proposed [14].

ANN has recently become a major tool in the field of microwave modelling and design [15, 16], and it has been used to reduce simulation time for SIW components, RF circuits, microwave devices, and circuits, all of which require more simulation time to optimize design parameters [17]. The design parameters of X band SIW H-plane bandpass filter have been optimized by using back propagation neural network (BPNN) proposed [18]. To optimize the SIW filter parameters, a novel neural network of calibrated coarse model has been proposed, and some training data have been used to synthesize the entire SIW filter [19]. To provide a quick and precise frequency response, the scattering parameter S_{21} in dB has been predicted using a multi-layer perceptron MLP-ANN [20]. A semi-supervised radial basis function neural network (SS-RBFNN) model has been proposed that uses an enhanced sampling strategy to reduce the uneven error distribution and slow convergence caused by sample selection uncertainty in the training process of artificial neural networks [21].

In this paper, a hexagon shape bandpass filter is proposed, and the filter parameters are optimized using MLP-ANN. Levenberg-Marquart (LM) algorithm is used to train the neural network. The keyword used is 'trainlm' in the MATLAB. The learning rate is 0.01, and the used activation function is log-sigmoid. The ANN results and CST Microwave studio simulated results are in good agreement.

This paper consists of five sections. The basic topology design methodology of proposed filter is explained in Section 2. The optimization of filter parameters using neural networks is explained in Section 3. The simulation results are explained in Section 4. The fabrication process and measurement setup are explained in Section 5.

2. DESIGN OF SIW BPF

The CST microwave studio is used to develop and simulate the hexagon-shaped bandpass filter depicted in Figure 1. The basic structure consists of three layers, and the bottom and top layers are perfect electric conductors (PECs). The middle layer of the SIW structure is made of Roggers RO4003C, which has a dielectric constant (ε_r) of 3.55 and substrate height (h) of 0.81 mm. The hexagon shape is modelled on the top PEC with a diameter (H_{dia}). Two square-shaped slots are etched on the opposite sides of the hexagon along the longitudinal direction. While microstrip feeding is given on both sides, these two square slots are used as feed points.

In order to make it as a SIW topology, the vias are arranged along the hexagon shape with a separation distance (p) and a diameter (d). From upper PEC these vias are penetrated through the dielectric material and the lower PEC. Two single layer Complimentary Split Ring Resonators (CSRR)

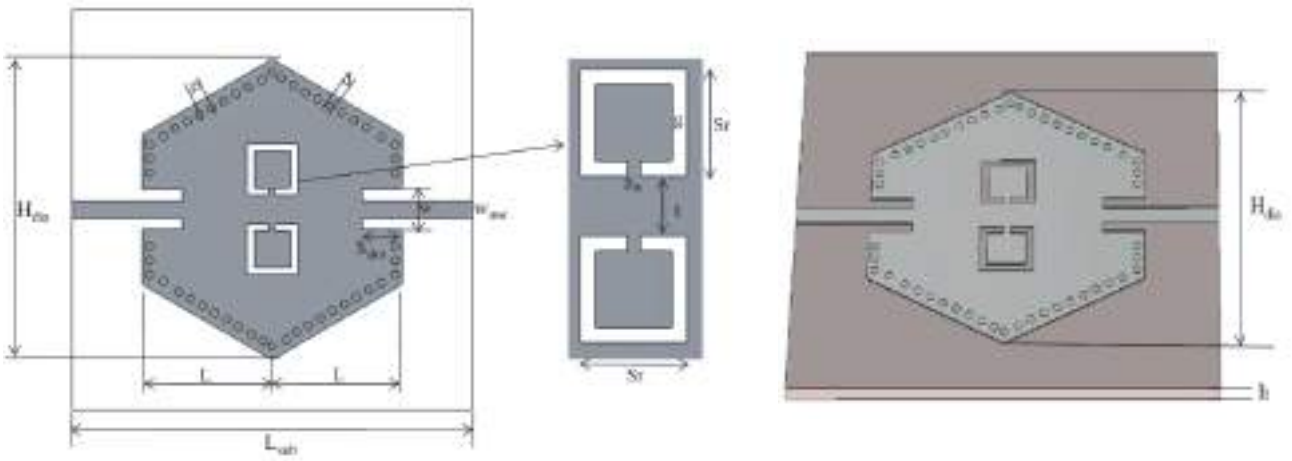


Figure 1. Topology of proposed filter.

are etched on the upper PEC. The optimised values for this hexagon shape topology are shown in Table 1.

Table 1. Dimensions of the proposed filter.

S. No.	Parameter	Value (mm)
1	d	0.8
2	H_{dia}	30
3	g	1
4	g_{in}	0.6
5	h	0.81
6	L	26
7	L_{sub}	40
8	p	1.4
9	S_{slot}	4
10	S_r	3.6
11	t	0.8
12	w	4
13	W_{mst}	1.74

3. BASIC MODEL OF BP-ANN

Neural networks play an important role in many engineering problems, so these networks are used in the filter parameters optimization. There are many types of neural networks available like multilayer feed forward neural networks (MLP-ANN), Temporal NN, radial basis function networks (RBF), Wavelet NN, and Self organizing maps [20]. Error back propagation multilayer perceptron artificial neural network (BP-MLP-ANN) is the most widely used network.

A neural network (NN) contains three layers, namely input layer, hidden layer, and output layer. The physical parameters that are intended to optimize are treated as input layer neurons. The second layer consists of a number of sub-layers which is known as the hidden layer, and finally, the output layer contains one or more neurons. Neurons are nothing but the information processing units, and they are also known as nodes or base points. The basic model of neural network is as shown in Figure 2.

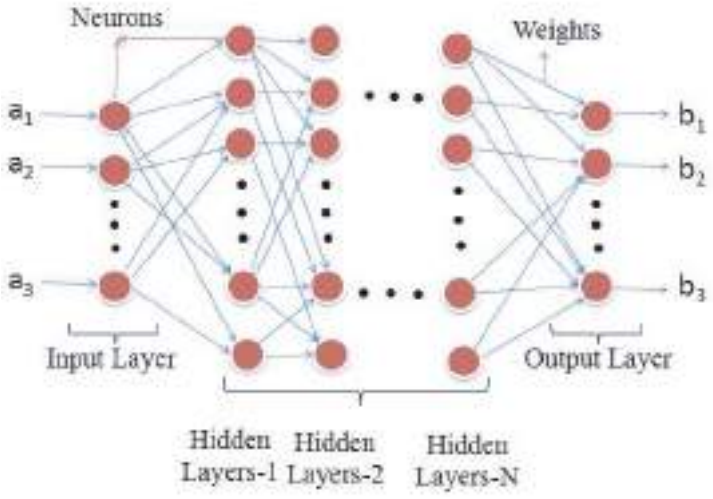


Figure 2. Basic model of Neural Network.

The links between neurons from input layer to output layer through the hidden layer are known as interconnections or weights.

In order to optimize the filter parameters, a supervised learning mechanism is used. In this method, the neural network must be trained with a set of known values, which are known as training data shown in Table 2, and this process is known as training of neural network. In the training process, the weights of the network are adjusted themselves to produce an output with a minimum mean square error (MSE). Now another set of data known as testing data shown in Table 3 is used to test the trained network. These two data sets are generated from the CST Microwave Studio by performing a number of simulations.

Table 2. Training data.

S. No.	S_{Slot} (mm)	S_{11} (dB) (CST)
1	3.95	−20.291
2	4.03	−19.616
3	4.05	−19.235
4	4.15	−17.367
5	4.18	−16.848
6	4.25	−15.921
7	4.35	−13.335
8	4.45	−12.448
9	4.55	−12.075
10	4.65	−11.233

Table 3. Testing data.

S. No.	S_{Slot} (mm)	S_{11} (dB) (CST)	S_{11} (dB) (ANN)	Mean Square Error
1	3.98	−20.415	−20.1313	0.2837
2	4.0	−20.673	−20.3526	0.3204
3	4.1	−18.276	−18.1666	0.1094
4	4.2	−16.670	−16.9877	0.3177
5	4.3	−15.004	−14.9313	0.0727
6	4.33	−13.598	−13.5915	0.0065
7	4.4	−12.863	−12.4525	0.4105
8	4.5	−12.078	−11.9968	0.0812
9	4.6	−11.622	−11.2806	0.3414

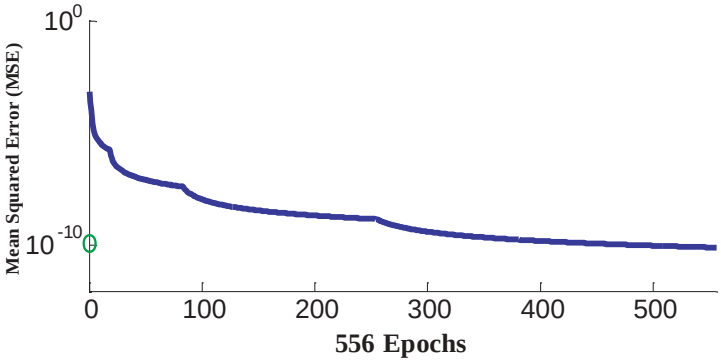


Figure 3. Training performance of the neural network.

The proposed neural network in this paper is a single hidden layer feed forward neural network, which comprises an input layer, a hidden layer, and an output layer, each having a number of neurons of 1, 10, and 1, respectively. The hidden layer neurons are fixed by trial and error method. Levenberg-Marquart (LM) algorithm is used to train the neural network. The keyword used is 'trainlm' in the MATLAB. The learning rate is 0.01, and the activation function used is log-sigmoid. Figure 3 shows the MSE plotted against the number of epchos, and the training performance of proposed neural network can be observed from this plot.

4. SIMULATION RESULTS DISCUSSION

The proposed hexagon shape dual bandpass filter, depicted in Figure 1, was designed and simulated using CST MWS, with simulated results presented in Figure 4. This graph shows the variation of S_{11} and S_{12} w.r.t frequency. The designed filter shows dual-band characteristics. The lower passband shows a narrow band response with a centre frequency of 10.41 GHz and offers a bandwidth of 403 MHz (ranging from 10.2 to 10.6 GHz). The proposed filter has another passband which is a wide-band response centred at 12.55 GHz. The upper passband provides a good wide-band response with a transmission bandwidth of 1.2 GHz (from 12.11 to 13.31 GHz). The return loss in lower passband is about −23 dB with a

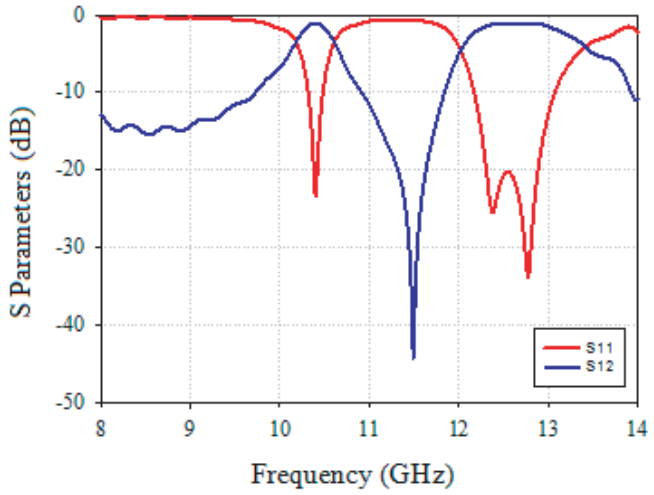
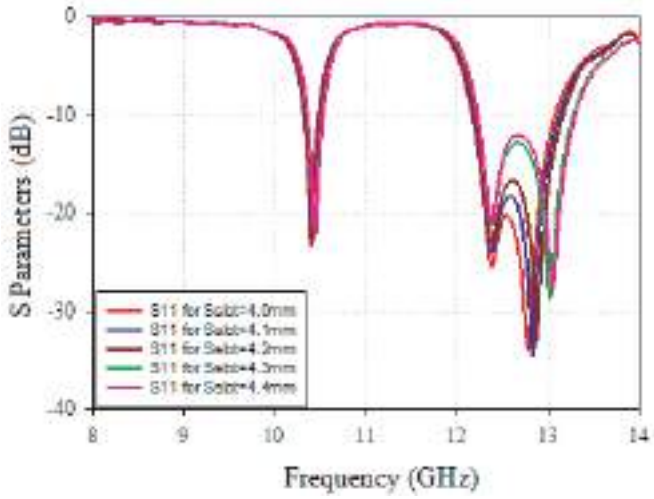


Figure 4. Frequency response of proposed filter.



(a)

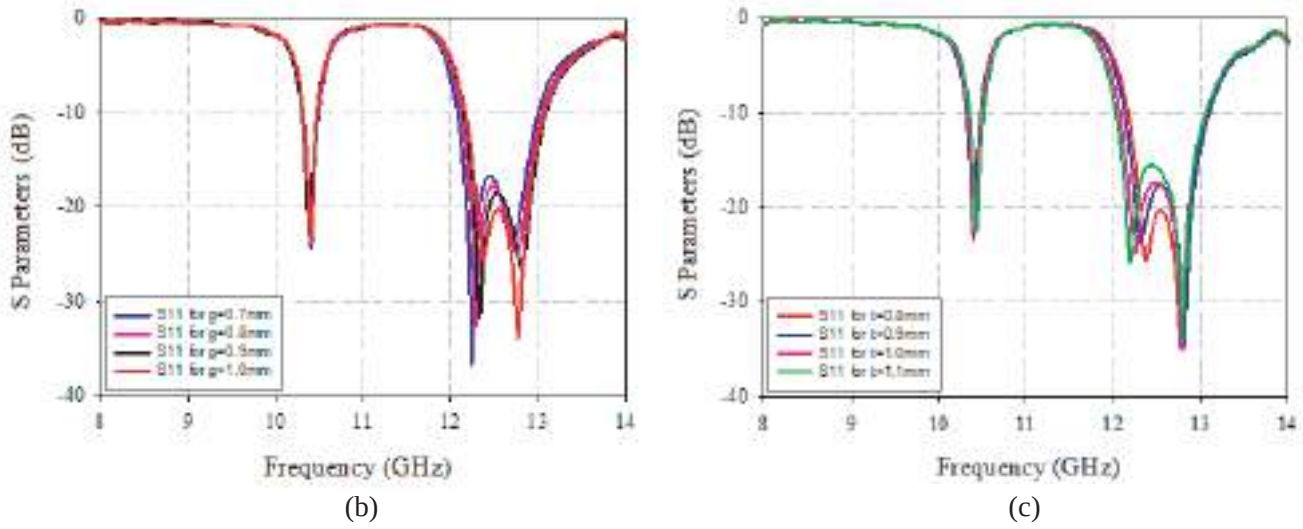


Figure 5. (a) Parametric analysis with respect to S_{slot}. (b) Parametric analysis with respect to 'g'. (c) Parametric analysis with respect to 't'.

fractional bandwidth of 3.84%, and in higher pass band it is about −20.4 dB with a fractional band width of 9.56%. Figures 5(a)–5(c) present the parametric analysis of the proposed filter. By varying different parameters like S_{slot}, g and t, the parametric analysis was carried out in order to generate training data for ANN.

Throughout the overall frequency band of operation, it offers an insertion loss of 0.8 dB. From the frequency response we can observe three transmission poles. One is at the first resonant frequency (fr_1) of 10.4 GHz in the lower passband, and the other transmission poles are in the upper passband at the second resonant frequency (fr_2) of 12.38 GHz and the third resonant frequency (fr_3) of 12.77 GHz. The electric field distribution of designed bandpass filter is shown in Figure 6 which is obtained in CST MWS while the simulation is carried out. The colour ramp represents the variation in electric field strength, and the proposed filter shows the dominant mode behaviour as normal rectangular waveguide.

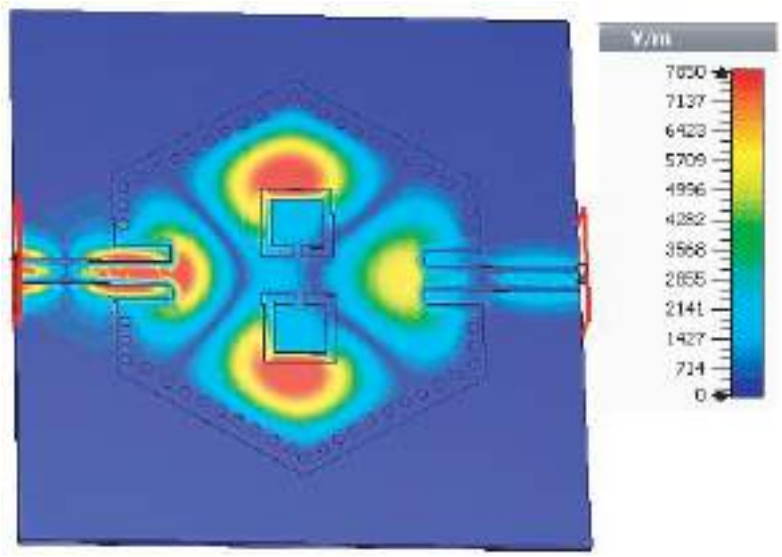


Figure 6. Electric field distribution.

5. FABRICATION AND EXPERIMENTAL VALIDATION

Figure 7 shows the fabricated model of the proposed filter, and Figure 8 shows the total measurement setup. Simple printed circuit board (PCB) process is used to design the proposed bandpass filter which shows two passbands. The dielectric substrate used is Rogers RO4003C of height 0.81 mm, having a relative permittivity (ε_r) of 3.55 and magnetic loss tangent tan(δ) of 0.0027. During the fabrication process of the proposed filter, at first the copper coating was done on both sides of the dielectric material. After that to make it into a SIW structure, via holes have been drilled. These via holes are placed in hexagon shape as shown in Figure 7. Finally from the upper PEC layer, a portion of PEC was removed in order to form CSRR slots. The Combinational Analyzer (Anritsu-MS2037C) has been used to measure this prototype model.

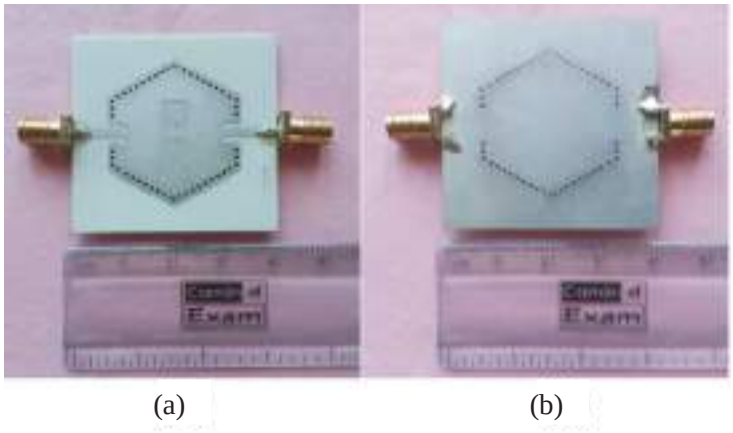


Figure 7. Photographs of fabricated models. (a) Top view. (b) Bottom view.

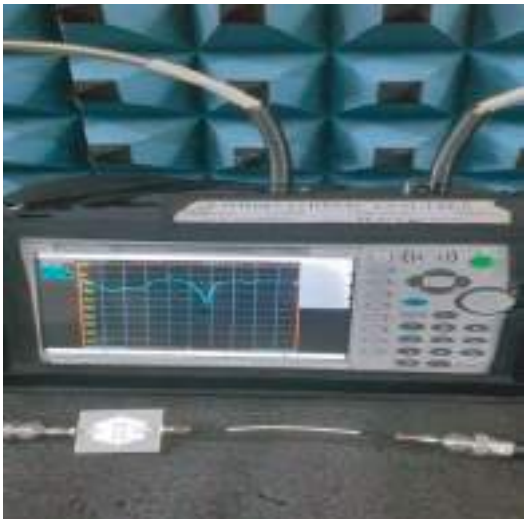


Figure 8. Measurement setup.

The measured results were plotted against the simulated ones, and they are in good agreement as shown in Figure 9. At -10 dB, in the lower passband and upper passband the measured S_{11} is shifted by 126 MHz and 90 MHz respectively from the simulated results.

From Figure 9, the simulated and measured transmission coefficients S_{12} show an insertion loss of

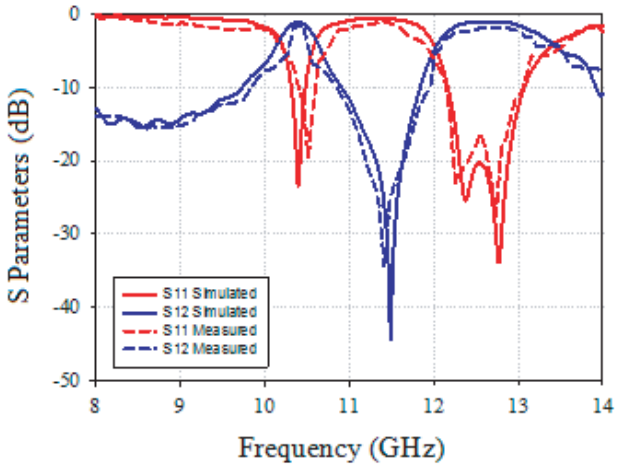


Figure 9. Simulated results plotted against measured results.

−0.8 dB and −1.55 dB, respectively, in the lower passband and upper passband which are about −0.8 dB and −1.62 dB, respectively. This difference in insertion loss is because losses due to SMA connectors were not considered while the simulation is performed.

6. CONCLUSION

A dual-band hexagon shape SIW bandpass filter with single loop CSRR based on ANN is presented. The design parameters of this filter are optimized by using an EBP-MLP neural network with LM algorithm and investigated using full-wave analysis with CST microwave studio. To prove the efficacy of the proposed model, a prototype is fabricated, and its functionality is verified experimentally. The measured insertion loss in the lower passband is about −1.55 dB and in the upper passband it is about −1.62 dB. The measured and simulated results are in good agreement and are also in good agreement with the ANN results with minimum mean square error. The properly trained neural networks give results at a faster rate than any other commercial CAD tools. The results are encouraging and useful for the easy optimization of SIW circuits with reduced computational complexity and execution time.

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NEW IOT ECOSYSTEM FRONTIERS - A SURVEY ON CLASSIFICATION IN TERMS OF IOT CHALLENGES AND CONSTRAINTS

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ABSTRACT

The way using the internet has been changed by the modern era; it is mutated into a strong enabler because it delivers customized ways to boost people's living standards. The Internet of Things (IoT) is a network of machines that can feel, connect with embedded technologies to meet, react to and help control their lives in all possible ways. Infrastructure availability, resource availability at inexpensive prices, IoT system usability at any time are the reasons for the enormous growth of IoT technology in the 21st century. It can be assumed that the IoT is the revolution that fuses the digital and physical world. COVID-19 is a pandemic disease caused by the Corona virus. It is a dangerous disease that in many countries has infected people and taken the lives of people in lakhs. It travels from person to person by the nose or mouth droplets of an infected person. As a protection against being poisoned, person to human contact must be prevented or adequate distancing must be preserved. In order to prevent the transmission of the disease, lock downs have been introduced. The year 2020 has created an opportunity to illustrate the role IoT has played in the lives of individuals from all industries. Anybody anywhere, anywhere linked to any aspect of the thing or part of the thing in this pandemic case. Anyone anywhere, everywhere related to any aspect of the thing or people around the world is made possible using IoT in this pandemic case. IoT and its classification are discussed in this paper

KEYWORDS: *IOT Ecosystem*

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INTRODUCTION

IoT interfaces gadgets and sensors through remote mode and make information accessible to the clients. The clients can get to and have control over the gadget from anyplace within the world. In straightforward words IoT performs AAA that's collect information, from any put any time anyplace at that point analyze, prepare information and perform activities to support the choice making. IoT interact within the same way how individuals connected in physical world. It is done with the assistance of computerized objects [1]. The advanced objects give information as physically given by the individuals for preparing. IoT replaces human- human communication. Agreeing to measurement report from Gartner IoT investigate, CISCO IoT solidness approximately 25-30 billion of IoT gadgets will be associated to the Web. It is evaluated that 127 modern IoT gadgets will be interfacing each moment. The number of IoT gadgets in domestic will have a fast rise and it is

anticipated to be around 12.86 billion. IoT has turned out to be boon not as it were for an indicated division but for all sectors [2].

There are two IoT markets. They are Even and vertical IoT showcase. IoT showcase which centres on the particular administrations that's in arrange to meet the requests of particular individuals is called vertical showcase and it may be either industry particular or statistic particular [3]. Level IoT showcase centres on wide extend of client needs and it has huge client base. In flat showcase buyers and buyers will be of distinctive divisions of the economy. From the Figure 1 it is obvious that sum contributed on vertical IoT of diverse divisions has seen fast development from 2015-2020. The number of IoT gadgets associated to the web is more than that of the versatile gadgets associated to web [4]. The assessed increment in showcase share contributed by diverse divisions towards IoT application for the year 2015-2025 is appeared within the Figure 2 and it is found that more speculations are made on wellbeing care units to convert conventional hardware and machines into savvy items. Since of this widespread COVID-19 there's plausibility to present Robots with wellbeing checking framework to dodge human interaction and to supply medications to tainted people to diminish the infection spread in future. So, rate of speculation in wellbeing care IoT applications will have colossal development when compared to other divisions. COVID-19 affect will cause a huge alter not as it were in Restorative IoT applications but too in instructive sectors as well as mechanical divisions where there's plausibility of interaction of community of individuals [5].

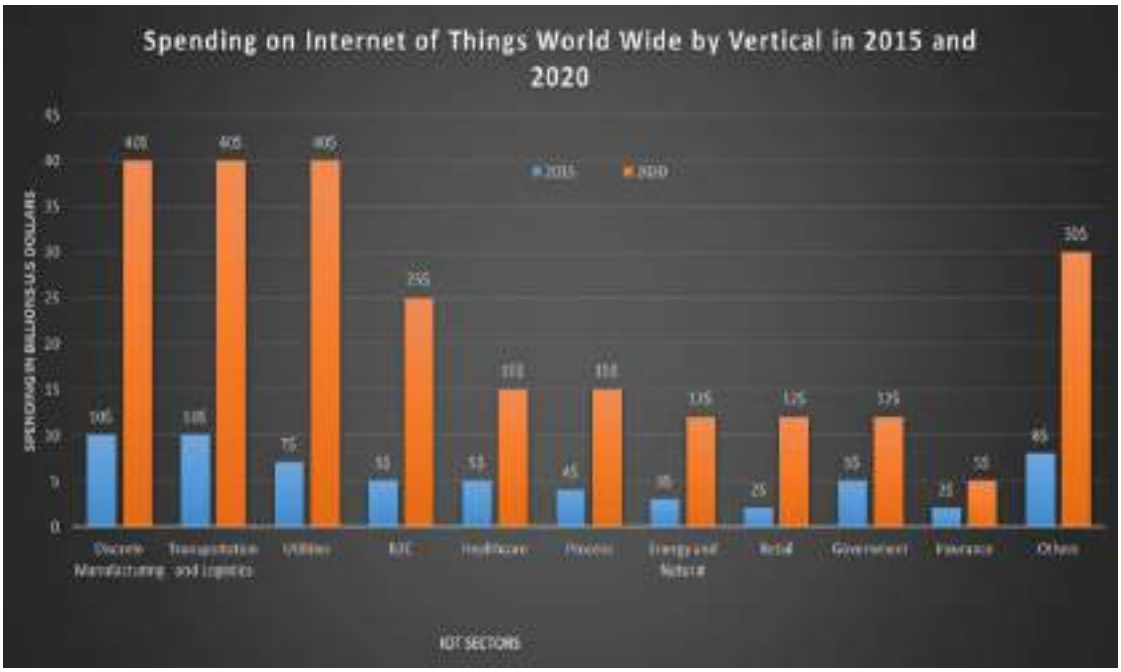

Figure 1: Investment in the Multiple IoT Industries in Billions of US Dollars (Source: Forbes).

IOT CLASSIFICATION BASED ON CAPABILITY AND PERFORMANCE

IoT grouping can be achieved in various ways. IoT gadgets are graded as low, middle and high-ended gadgets on the basis of capability and execution. Low-end gadgets based on advanced features such as memory, backup of heterogeneous devices, network organization, reliability and genuine time capability are categorized as Type0, Type1 and Type2. Cameras, actuators, openmote, waspmote, Tmote sky, ATMEL SAM R21 Xplained-pro, etc. Type0 has resources that are minimal. The first layer reflects it. It contains functions for sensing and actuating. In contrast to low end instruments, Sensors Type1 has more power [6]. It offers more features than Type0.0. The downside is that it has little computational capacity to manage difficult specifications. It requires fundamental microcontrollers. In other words, it increases the

functionality of IoT products with lower ends. It has functions such as image recognition, extraction of data, etc. Form 2 requires CPU, RAM, flash memory and supports traditional operating systems such as LINUX, UNIX. It can be combined with nearly all protocols for communication. The ability of middle-end IoT systems to use more than one communication technology. The spectrum of hundreds of MHZ is the clock speed and RAM [7]. It has more limited resources relative to low-end devices, but fewer than those of high-end devices. The design specifications for IoT devices and protection requirements for these IoT devices are outlined in Table 1 and 2.

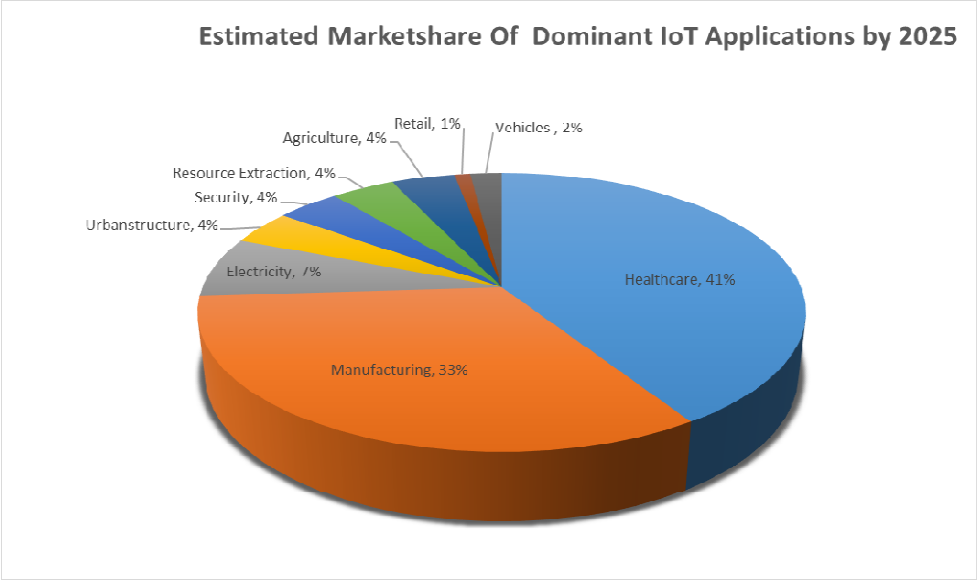

Figure 2: Estimated Contribution of the IoT Industries that Control.

Table 1: Specifications for Various IoT Application Forms

	Specifications				
		RAM	**Flash**	**RTOS Support**	**Communication Protocols**
Low End Devices	Type0	<10kB	<100 kB	Does not support	Use gateways for communication No protocol stack embedded
	Type1	~10kB	~100kB	Could be implemented	Use light weight protocols, communicate with other devices without using gateway
	Type2	~50kB	~250kB	Could be operated	Supports communication protocol such as HTTP

Table 2: Security Specifications Focused on the Capability of IoT Devices

Categories	**Security Requirements**	**Type0**	**Type1**	**Type2**
Confidentiality	Message encryption		Yes	Yes
	Malware response			
	Data encryption		Yes	Yes
	Tamper resistance		Yes	
	Device ID management	Yes	Yes	Yes
Integrity	Data integrity		Yes	Yes
	Platform integrity			Yes
	Secure booting			Yes
Availability	Logging		Yes	Yes
	State Info. Transmission	Yes	Yes	Yes
	Security monitoring			Yes
	Security patch			Yes
	Security policy			Yes
	Software safety		Yes	Yes

Table 2: Contd.,

Authentication/ Authorization	User authentication		Yes	Yes
	Device authentication		Yes	Yes
	Password management		Yes	Yes
	Access control		Yes	Yes
	Device ID verification			Yes

IOT GROUPING BASED ON THE LIFE CYCLE OF ORGANIZATION AND OPERATION

Another grouping, based on the association of the entity with that of physical equipment, is known as low-level operation, assets service, entity service, consolidated service [8]. IoT is defined as deployable, deployed, or operational, depending on the level of service. Figures 3 and 4 reflect the classifications.

IOT GROUPING BASED ON OPERATING SYSTEM

A series of programs called the operating system is a bridge between applications or users and computers. The operating system is built on the IoT computers to run the programs and control the devices. It is further graded as low and high-end depending on the operating system (OS) [9]. In figure 5, the schematic representation is shown. Table 3 displays some of the operating systems required for low-level and high-level computers.

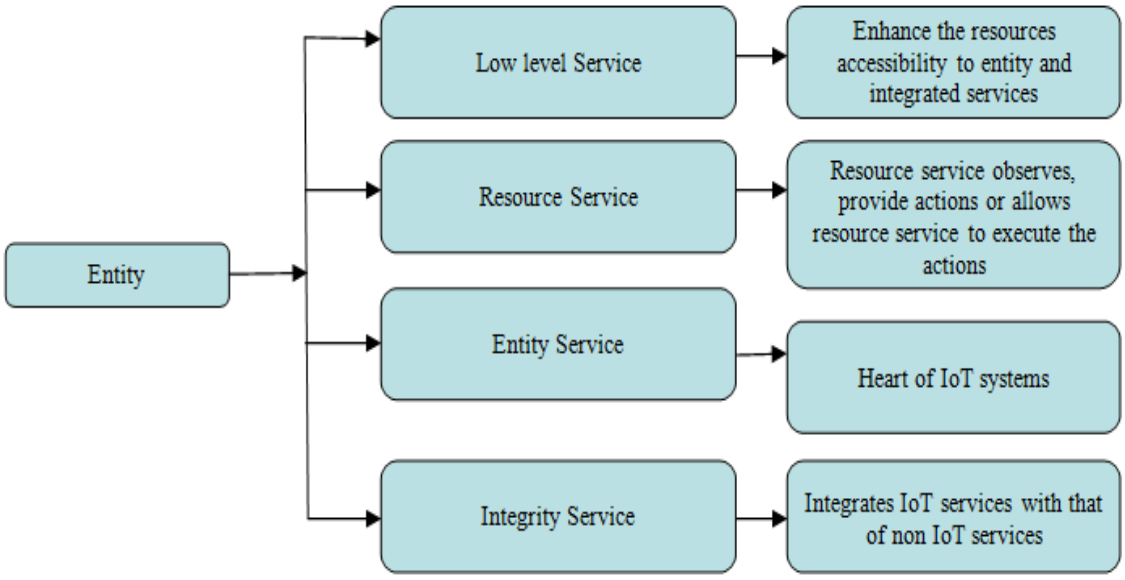

Figure 3: Entity Partnership Definition Based.

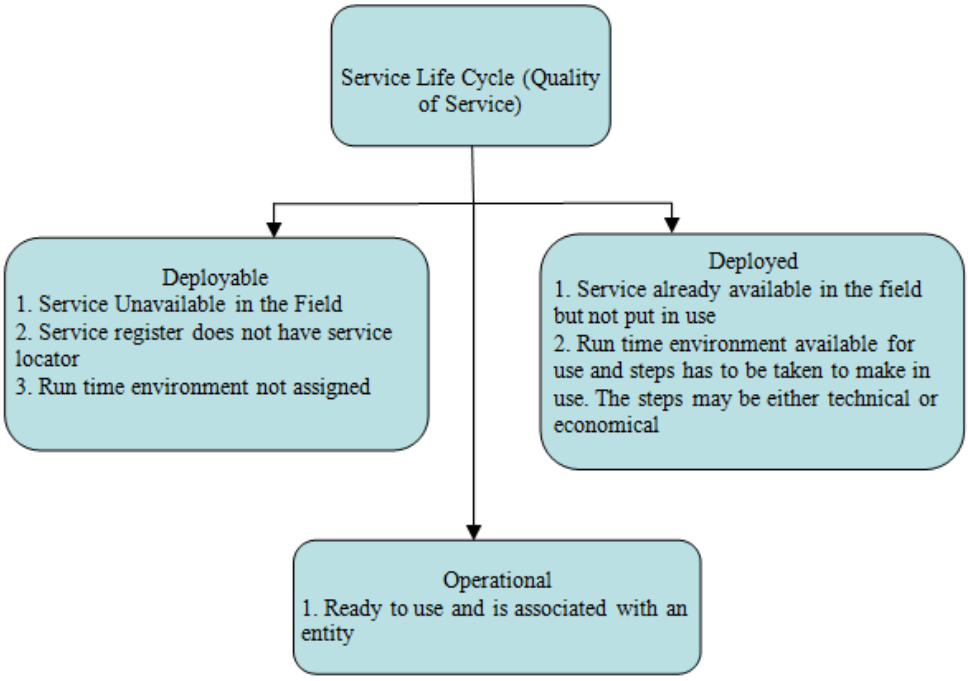

Figure 4: Operation Life Cycle-Based Grouping.

Table 3: OS for Device with IoT

Operating System	Supporting Device	IoT-Enabled Devices	OS Supporting
Tiny OS	No	Low	Non-Linux
Contiki	Yes	Low	Non-Linux
RIOT	Yes	Low	Non-Linux
LiteOS	No	Low	Linux
FreeRTOS	Yes	Low	Non-Linux
Mynewt	Yes	Low	Linux

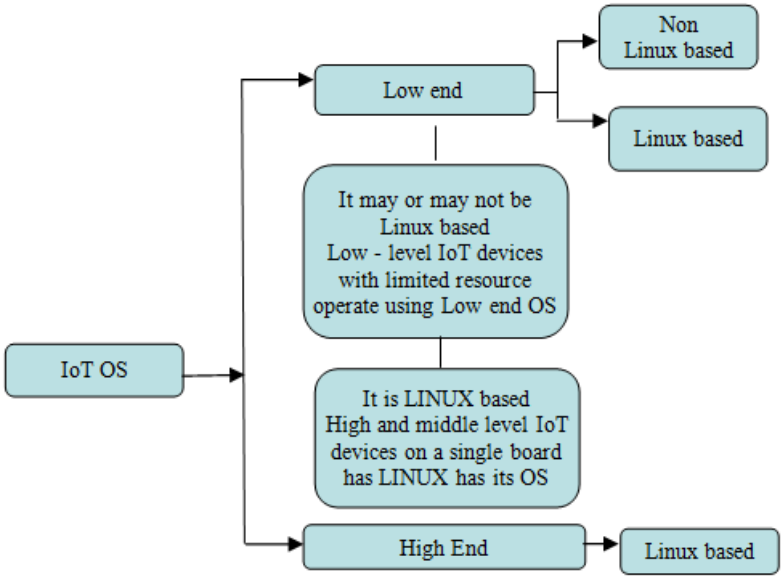

Figure 5: Classification by Type of OS Used.

IOT GROUPING BASED ON NETWORKING TECHNOLOGY

To provide basic smart services, IoT requires connectivity technologies to connect heterogeneous objects. In the sharing of information, communication technology support. It is possible to connect locally using Bluetooth, NFC or the Internet [10]. The key distinction between local and internet protocol communications is focused on variables such as transmission range, power usage, and memory used. IoT includes networking technologies to connect heterogeneous objects in order to provide simple smart services. Communication infrastructure assists in the exchange of knowledge. Bluetooth, NFC or the Internet may be used to connect locally. Variables such as propagation range, power consumption, and memory used reflect on the main difference between local and internet protocol communications. A subclass of RFID is NFC. NFC is a 13.56 MHZ high frequency RFID. RFID is a protected method of data sharing, consisting of a reader, tag and antenna. RFID may either be passive or aggressive. There are variations between Active and Passive RFID in Table 4.

Table 4: Active and Passive RFID

Active RFID	Passive RFID
It has own power source	Do not have their own power source
It finds its application in construction, security, Public works	It finds its applications in paper, textile etc.
Tags are costly and have limited life span	It is small size, light weight and has long life span

Low Power Technologies- Developed Low Power Technologies to support the IoT model. The arrangements for all forms of sensors are improved by LPWANS (Low Power Large Area Networks). With thin, cheap batteries lasting for years, it has the potential to provide long-range communication. It finds its applications in remote controls, smart meters, construction contracts, etc. Registered versions such as NB-IoT, LTE-M and unlicensed versions such as MYTHINGS, LoRa, Sigfox and so on can be used. Reliable broad band connectivity is provided through wireless technologies used in mobile phones [11]. For its service, it needs power and its operating cost is high. Due to factors like frequency, contact range and security, it does not support most IoT products. Due to high energy demand, Wi-Fi finds its applications in intelligent home appliances, surveillance cameras, etc. Coverage, scalability and power usage are the considerations that make it less widespread. Wi-Fi-6 offers increased bandwidth < 9.6Gbps to improve data transmission in order to address the data transfer caused by the congested environment. Wi-Fi HaLow has enhanced energy output but lacks security. Along with electronic sensors, blue tooth low energy and blue tooth devices are used to provide a smart interface specifically for medical wearables and exercise. The topology of Mesh helps Zigbee to connect with more IoT computers. Higher data rates are enabled and less electricity is used. It finds its applications in medium-range IoT devices such as energy management, protection, HVAC control and so on due to low power consumption. For all IoT programs, the network specifications are not the same [12]. Each IoT application has a prerequisite for its own network. Availability, security, bandwidth latency, power consumed by devices, service quality, network management are the factors that affect the selection of wireless technology for specific IoT applications. The wireless technology for different IoT implementations is seen in Table 5.

Table 5: For Separate IoT Verticals, Wireless Technology

Key IoT Verticals	LPWAN (Star)	Cellular (Star)	Zigbee (Mostly Mesh)	BLE (Star & Mesh)	Wi-Fi (Star and Mesh)	RFID (Point-to-Point)
Industrial IoT	Highly applicable	Moderately applicable	Moderately applicable			
Smart Meter	Highly applicable					
Smart City						
Smart Building			Moderately applicable	Moderately applicable		
Smart Home			Very High	Very High	Very High	
Wearables	Moderate			Very High		
Connected car					Moderate	
Connected Health		Highly applicable		Highly applicable		
Smart Retail		Moderately applicable		Highly applicable	Moderately applicable	Highly applicable
Logistics & Asset tracking	Moderately applicable	Highly applicable				Highly applicable
Smart Agriculture	Highly applicable					

IOT GROUPING BASED ON MIDDLEWARE

The computing layer called IoT Middleware connects various application domains to interact over different domain interfaces. Middleware is often referred to as software glue because it allows software engineers to build contact implementation programs. If complex programming is not designed initially middleware enables to integrate it later with the help of support architecture. Schematic representation of the general functions that middleware executes [13]. In order to identify IoT middleware as service-oriented, cloud-oriented and actor-oriented middleware, accessibility, versatility and adaptive design are used. Service-oriented middleware- For end users, developers, extension and modification of IoT devices is allowed. Standalone or cloud storage systems can be service-oriented. Since it is not cost-effective, it does not support homogenous framework deployment. To support constrained services, there is no architecture provision for security techniques. Cloud-oriented middleware, which conveniently captures data, analyzes and interprets data. Security and privacy cannot be configured by the user. It has autonomy over critical details, but to support limited capital, it has no architecture framework. Users are permitted to plug and play IoT devices with actor-oriented middleware. They will uninstall the specific IoT device without disrupting and impacting the other elements of the IoT environment whenever the consumer does not need an IoT device. It enables protection and privacy to be configured by the user. Middleware is also defined as service-oriented, node-based, component-based, clustered, distributed, client-server, based on architecture nature.

IOT GROUPING BASED ON DESIGN

The simple IoT architecture consists of only three layers, namely perception layer-performing sensing and actuating, network layer-performing data transmitting and processing, device layer-providing the necessity to the user. Additional layers are used in the five-layer architecture to provide additional abstraction to the IoT architecture. Middleware interconnects heterogeneous objects with the heterogeneous device is the back bone of the IoT ecosystem, involving perception-where sensor tests the data, transport layer-performs transporting data function, processing layer-process and evaluating the data collected through transport layer. Through having control over the data flow, Middleware controls the

system. The sensors and actuators have the vision layer in the middleware-based architecture along with the access layer and edge layer. The Coordinate layer provides the customer with a final application along with the application layer. Data objects in service-oriented architectures are extracted and exposed through interfaces. While the technologies and the cloud differ, the Application Programming Interface (API) stays the same. The physical layer is often the bottom in fog-based architecture, the next layer is monitoring-observing and testing the data obtained from sensors. The pre-processing layer processes the data for processing-based results. In order to provide data protection and privacy, the security layer is liable. Perception layer-Includes actuators and sensors. Sensors track the physical and environmental parameters, gather certain parameters, erase the undesirable data and transfer the data to the actuators in order to execute actions. Transport layer-Utilizing communication protocols like Zigbee, BLE, NFC etc., brings the preprocessed data for processing to the processing layer. Processing layer- Filter, formatting information gathered from sensors. It also stores and handles, via communication protocol, the sensed data received from different devices. Middleware layer- To provide useful information, it conducts conceptual and analytical operations on the data available. It uses computing platforms and cloud storage. The application layer provides the user with an application using communication protocols such as MQQT, Restricted Application Protocol, and (CoAp). IoT architecture is shown in Figure 6.

Table 6: Design of IoT

<table>
<tr><td rowspan="2">Application Layer</td><td>Application Layer</td><td colspan="2">Application Layer</td><td>Applications</td><td>Transport Layer</td></tr>
<tr><td rowspan="2">Middleware Layer</td><td colspan="2" rowspan="2">Coordination Layer</td><td>Service</td><td rowspan="2">Security Layer</td></tr>
<tr><td>Composition</td></tr>
<tr><td rowspan="2">Network Layer</td><td rowspan="2">Processing Layer</td><td colspan="2" rowspan="2">Middleware Layer</td><td>Service</td><td rowspan="2">Storage Layer</td></tr>
<tr><td>Management</td></tr>
<tr><td>Perception</td><td rowspan="2">Transport Layer</td><td colspan="2" rowspan="2">Backbone Network Layer</td><td>Object</td><td>Pre-processing</td></tr>
<tr><td>Layer</td><td>Abstraction</td><td>Layer</td></tr>
<tr><td></td><td rowspan="2">Perception Layer</td><td>Perception</td><td>Access Layer</td><td rowspan="2">Objects</td><td>Physical Layer</td></tr>
<tr><td></td><td>Layer</td><td>Edge Layer</td><td>Physical Layer</td></tr>
<tr><td>Three Layer</td><td>Five Layer</td><td colspan="2">Middleware based</td><td>Service oriented Architecture</td><td>Fog based</td></tr>
</table>

IOT PLATFORM GROUPING

The IoT interface bridges hardware and technology. The IoT platform is a feature of middleware that links gateways, cloud, server and device networks. Infra layer-performs intercommunication between devices, messaging feature, connection layer-enables communication between hardware and cloud to transfer data for data analytic processes, core layer-collects data, identifies the device, manages the device, updates the software framework. From the produced reports, the results can be calculated. To process the data, it frames the rules. Reports are created based on the rules applied. This layer connects the network, the gateways, to the cloud or device layer.

CONCLUSIONS

Because of the Internet and the apps generated on the internet, the environment has changed the way we work, move and do business. The Internet is predominantly based on a totally beneficial growth. Without IoT, contact turned out to be unlikely in all cases. IoT will change everything and is the cornerstone of a modern technological transformation, referred to as Business 4.0. It is the secret to organizations, cities and culture as a whole being digitally changed. A variety of sensors are built into the IoT. By having communication between smart devices, the IoT has the ability to extend its visibility. These systems are fitted with features such as identification, sorting, interaction, networking and service. Due to their small nature, less weight and cheap use of sensors and actuators is omnipresent. This paper provides an overview of the emerging IoT based on power and performance, organization, life cycle based on operation, operating system,

infrastructure, storage of middleware, portal, network, technologies of communication, applications. In order to improve people's convenience and quality of life, a series of technologies are involved. In order to face the difficulties that occur as vast quantities of data are managed by the IoT, research needs to tackle key problems such as stability, anonymity, scalability, interoperability, mobility and availability.

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A STUDY OF BANDWIDTH CONSUMPTION GAINSFOR IMPROVING SMART GRID QoS

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ABSTRACT

Recently, the smart network performance is great significance in quality of service. When the Energy server provider requires several types of information signals with different requirements from all nodes it manages. these signals will meet some interference when sent in view of the limitation of bandwidth for wireless technologies. To insure from receiving information signals its required suitable modulation schemas Proportional to hugging data signals whereas any wireless communication technology performance depends firstly on bandwidth factor and latency. This paper explains bandwidth consumption gains (BCG) to match the appropriate communication technologies that enhance the QoS of Smart Grid.

KEY WORDS: *Smart Grids, Different Communication Technologies,Bandwidth, Latency Factor, Different Nodes, Bandwidth Consumption Gain (BCG), Energy Service Provider (ESP).*

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ORIGINAL RESEARCH PAPER

Computer Science

IOT BASED APPLICATION CASE-STUDY FOR TRANSMISSION OF SLEEP APNEA PATIENT VIDEO WITH SOUND

KEY WORDS: sleep apnea, video, audio, mobile

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ABSTRACT

Mobile video-audio transmission systems have delivered patient video with relevant snoring sound to quantify the severity of the sleep apnea patient over wireless networks, but few have optimized video-audio transmission in combination with transmission protocol over error-prone environments using wireless links. In this paper, the performance of the MPEG (Motion Picture Expert Group)-4 error resilient tools with UDP(User Datagram Protocol) protocol were evaluated over a wireless network to suggest the optimum combination of MPEG-4 error resilient tools and UDP packet size suitable for real-time transmission of video-audio transmission over error-prone mobile networks. Through experimentation, it was found that the packet size should correspond to IP(Internet Protocol) datagram size minus UDP and IP header for optimal video-audio quality. Also, for error resilient tool selection, the combination of resynchronization marker and data partitioning showed the best performance.

INTRODUCTION

Advances in mobile communication technology have enabled the access of patient video-audio information without the limitations of time or location. Mobile technology can offer continuous, uninterrupted, and instant service to ultrasound application domain. However, the current bandwidth of the mobile network is not sufficient to transfer patient video data requiring high throughput. Besides the bandwidth of the mobile network, the high error rates due to multipath fading should be taken into consideration to sustain, video transmission in mobile transmission systems [1].

MPEG-4 has been successfully applied to many types of mobile applications [2]. Some pioneering telemedicine applications of MPEG-4 can give insight into the compression efficiency for patient video streaming over the limited bandwidth of the mobile network [3,4]. However, the error resilient tools of the MPEG-4 standard, which are important for error-prone mobile applications, have rarely been researched, particularly for use in mobile transmission applications. In addition to compression, an efficient data transmission protocol should also be considered for real-time video streaming. Between the two well-known network protocols, TCP(Transmission Control Protocol) and UDP(User Datagram Protocol), UDP is much more suitable for real-time streaming because it uses simple datagrams with no congestion control [5]. Nevertheless, little research has been conducted to comprehensively validate the efficacy of the MPEG-4 error resilient tools in combination with the UDP protocol when applied to a mobile video-audio system.

ERROR RESILIENCE IN MPEG-4

MPEG-4 [2] provides error resilient tools to enable robust transmission of compressed ultrasound video over error-prone mobile networks, which are subject to Rayleigh fading and burst errors as a result of multipath propagation [6]. MPEG-4 employs four types of error resilient tools to enable resynchronization, error detection, data recovery, and error concealment: resynchronization markers (RMs), data partitioning (DP), reversible variable length coding (RVLC), and header extension code (HEC).

EXPERIMENTATION

Data Transmission Format

An MPEG-4 bit stream composed of a series of video packets is encapsulated into an IP datagram using the UDP protocol. As shown in (Fig. 1), an IP datagram consists of UDP data corresponding to the fragmented MPEG-4 bit stream data, 8 bytes of UDP header and 20 bytes of IP header. A total of 28 bytes of overhead is created by the attached headers [5]. Particularly, the UDP protocol drops the whole UDP datagram when corruption of the UDP datagram is detected by the checksum field within the UDP header.

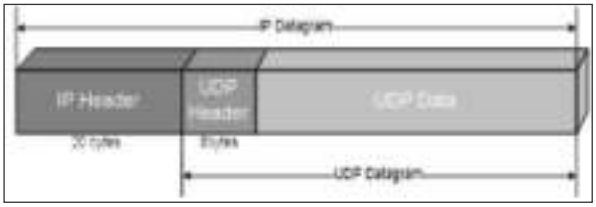

Fig. 1. Encapsulation Of A UDP Datagram Within An IP Packet

Experimentation

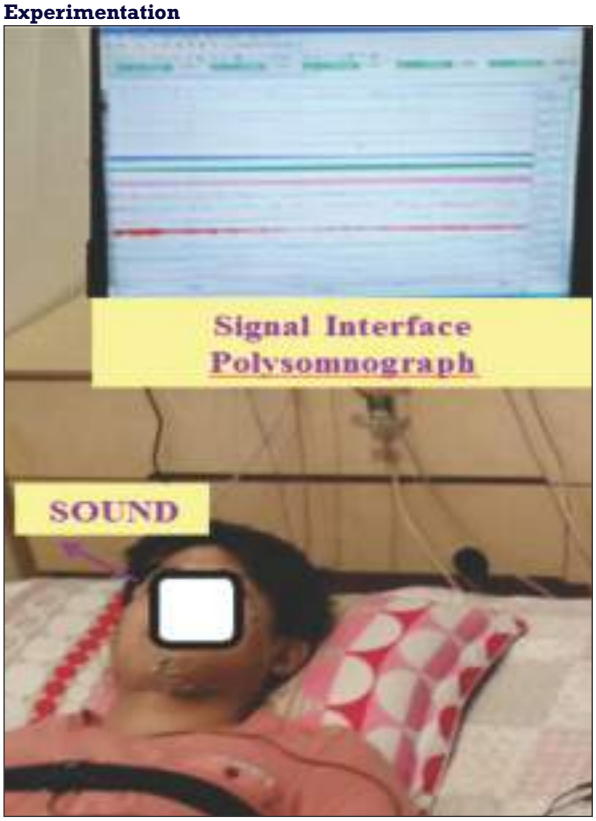

Fig. 2. A Typical Image Extracted From A Patient Video With Audio And Signals Interface For Experimentation

Measurements were taken for 7 days at the Seoul metropolitan area. As shown in (Fig. 2), 30 seconds of captured video-audio were repeatedly used for each measurement. The output bit rate of the MPEG-4 encoder (spatial resolution of 320x240, frame rate of 4 frames/sec, and key-frame period of 2 sec) was set to 80 Kbps, considering a measured mean bit rate of 100 kbps for the reverse link [7] and an MPEG-4 decoder buffer margin of 20 kbps for network jitter compensation. Because of the interrelation between the error resilient tools (for example, RVLC should only be used in conjunction with DP), and the header's relative importance compared to other streaming data, three different combinations of error resilient tools were considered, all utilizing HEC: RM only, RM with DP, and RM with both DP and RVLC. At the MPEG-4 decoder, an error concealment technique was employed before evaluating video quality. In particular, when the frame drop occurred due to a burst error, the dropped frame was replaced by the previous frame. The MPEG-4 simple profile with error resilient tools was implemented by mpegable Video SDK (Dicas Co., Germany) [8].

RESULT

In order to analyze the error effect of the wireless networks with respect to different IP datagram sizes (corresponding to UDP datagram sizes), the IP datagram size was varied between 200 and 5000 bytes. As shown in (Fig. 3), the DLR increased as IP datagram size increased, because UDP discards the entire datagram regardless of the amount of corruption when an error is detected within. As the size of the IP datagram increased, the percentage of UDP data increased relative to the headers (with a fixed size of 28 bytes), Thus, PSNR increased as the size of the IP datagrams increased.

When the compressed bit stream is not contaminated by error (before transmission) as shown in (Fig. 4a), the highest PSNR can be obtained without using any error resilient tools. Moreover, the PSNR decreases as more MPEG-4 error resilient tools are employed. (The use of headers is unavoidable if any error resilient tool is employed.) Thus, for fixed-size bits, the bits allocated for a patient video can be decreased if the bits allocated for headers are increased. Particularly, the abrupt change in PSNR for the case using RM with both DP and RVLC is due to fact that the prefix for RVLC requires additional space compared to RM and DP.

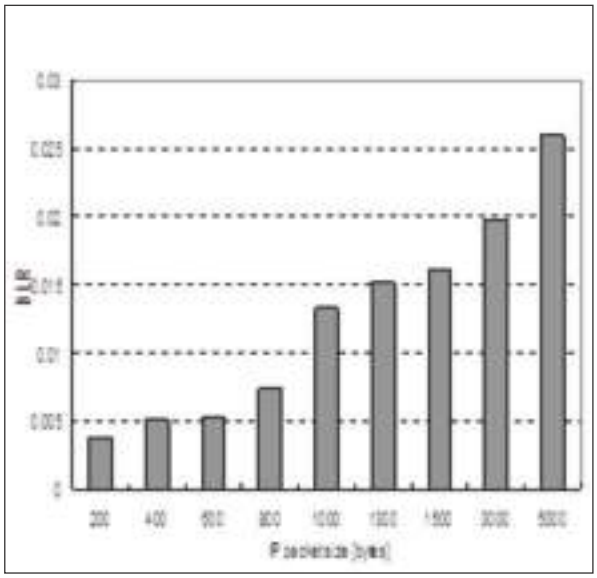

Fig. 3. Datagram Loss Rate (DLR) In Terms Of IP Datagram Size After Mobile Transmission

CONCLUSION

The selection of an appropriate error resilient video compression method might be a primary concern in designing a mobile video-audio transmission system running over a mobile network with limited bandwidth. Among the many standard video compression methods available, MPEG-4 can be regarded as one of the most appropriate for compressing video data for transmission over a mobile network, because MPEG-4 offers high compression at a low bit rate and useful error-resilient tools [6]. In addition to the compression method, a transmission protocol, either TCP or UDP, should also be taken into consideration when transmitting a compressed bit stream over an IP-based mobile network [9]. For real-time video-audio transmission over an error-prone mobile network, the conditions required to select the transmission protocol are the capability for real-time streaming and tolerance to frame loss [10].

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An Advanced Filter Topology and Effects for compensating common Mode Voltage in Vehicular Induction Motor Drives

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Abstract: Recently the utilization of electric vehicle technology increasing drastically, because of environmental changes arises throughout the globe. Based on these issues, this paper focuses on the drive used in the electric vehicle with more economically. In general electric vehicles the induction motor drives are used, because they have great features, such as high starting torque and high efficiency. The motor drive is driven by the high switching frequency PWM inverter supplied by a dc source or supply, because of this switching frequency common mode (CM) voltage generated at the input of stator motor terminals, creating a shaft voltage through the motor air gap with possible rise in bearing current, leading to premature damage to the motor reliability and lifetime. To compensate this problem an advanced active filter is designed, which will suppress the common mode voltage. And also analyze the impact of electromagnetic interference (EMI) on drive under the test (DUT). The above system will initial executed in the electrical software tools like MATLAB/SIMULATION for confirmation of the results, suitable for electric vehicle applications, especially for induction motor drives.

Keywords: Common mode (CM) voltage, Shunt active filter, Electromagnetic Interference (EMI), Induction Motor drive.

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I.INTRODUCTION

In the present applications of electrical vehicles, high quality output is achieved through the pulse width modulation (PWM) IGBT switches. It creates high switching frequency at the inverter output terminals and generates common-mode voltages at drive input side. This common mode voltage produces shaft voltage therefore produces bearing currents through stray capacitances. Amplitude of the shaft voltage and bearing current influence the electromagnetic interference (EMI) problems. It also leads to severe damage to the insulation of the motor i.e. life time and reliability of the motor [1].

Several literatures exhibit that the suppression of the common mode voltage in the induction motor drive fed by high voltage dc supply [2-4]. They have proposed the common mode active filters to mitigate the common mode voltage at the input motor terminals. Two kinds of methodologies are proposed to synthesis the common mode voltage, one of them is the passive circuitry [5], it consists of simply resistors, inductors, capacitors and common mode chokes. The values of those parameters are depending on the length of the cable from inverter and motor [6]. The second methodology is used to mitigate the common mode voltage on the inverter fed induction motor drive with an active circuitry. This is the one of the most effective processes used in the industrial drives in the last five years. Generally, it eliminates the mirror image of common mode voltage, i.e. shaft voltage and the bearing currents [7-10]. This active circuit canceller contains different parts for detection and reinjection of the voltage in the line, this detection circuit consisting of star connected capacitors, Darlington pair of transistors, a four winding transformer and additional dc power supply. This circuit focuses on the common mode voltage detection at the inverter output, transfer of the common mode voltage by a voltage follower amplifier to a common mode transformer and reinjection of the compensated voltage through CMT [11-15].

In this paper, a dc power supply of 575V is derived from an ac power supply for reduction of the cost. This is proposed for the suppression of common mode voltage and thereby shaft voltage and bearing currents will be reduced. The proposed methodology is simulated using MATLAB and executed experimentally further.

A high frequency model induction motor is used throughout the simulation. According to the CISPR model, a dedicated 600V high voltage dual-LISN [16-17] is designed and built for the simulation, Also concentrated on the active common mode voltage canceller (ACMVC) for compensating the common mode voltage. The present literature represents that the emitter follower realized by transistors (at present, bipolar p-n-p transistors with more than 400V are not available) instead of MOS-FET transistors

are implemented in this investigation. The proposed methodologies are supposed to be implemented in electric vehicles, hybrid electric vehicles, plug-in hybrid electric vehicles and fuel-cell vehicles that improves the overall system reliability and also reduces the cost and size.

This paper is organized in different sections, introduction of the work is presented in section I. In section II, the design considerations of the high voltage dual channel Line impedance stabilization network (LISN), standards for comparison of results with the CISPR, circuit configurations, mathematical design features are explained. Section III describes design considerations for high frequency induction motor model to make it suitable for measurement of common mode ground currents, and its equivalent circuits with values. In section IV, design features for the common mode voltage active canceller (CMVAC), its circuit configurations, and CMT are described. Section V describes the results obtained in simulation. The outcomes of the work are concluded in section VI.

II. LINE IMPEDANCE STABILIZATION NETWORK DESIGN CHARACTERISTICS

The Line impedance stabilization network is a low pass filter placed between AC or DC power source and the equipment under test (EUT) to create known impedance as per complying standard for the measurement of conducted emission. This provides a Radio frequency (RF) noise measurement port. It also isolates the unwanted RF signals from the power source when pre-filter is included. Specifications of The LISN are presented in Table 1.

The LISN is generally used in the repeatable and accurate measurements of the conducted emissions generated by the high switching frequency inverters. Two identical LISNs are placed in the same metal structure (line and neutral). As per the standards of CISPR, the values of the line and neutral LISNs are inductance (L) of 5μH, capacitor (c1) with 1μF on the mains side. A 50Ω resistance, output measuring instrument, and coupling capacitor c of 0.1μF are placed on the drive under test side (DUT). [19-20],

The Figure 1 shows the circuit model of the high voltage dual channel LISN, which is built on dedicated earthing. More or less each of LISN must meet the standard impedance curve defined by CISPR16-1[20-21] as shown in Figures 2-4. And also the ideal impedance curve and measured impedance curves at the line and neutral are represented in Figure 2, Figure 3, and Figure.4. These curves are measured by Rohde and Schwarz vector network analyzer ZVRE.

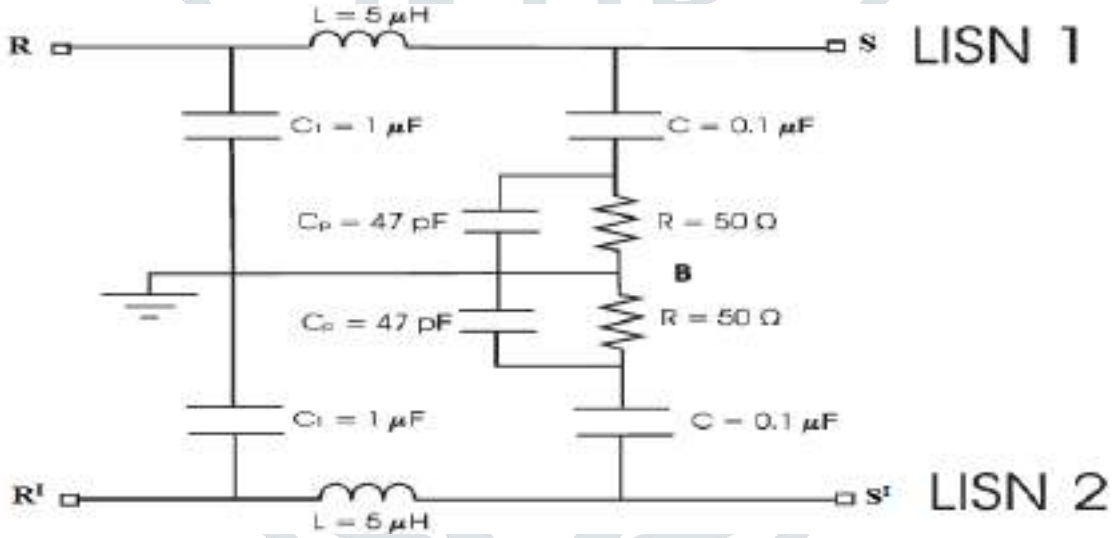


Fig: Circuit model of high voltage dual Line Impedance Stabilization Network

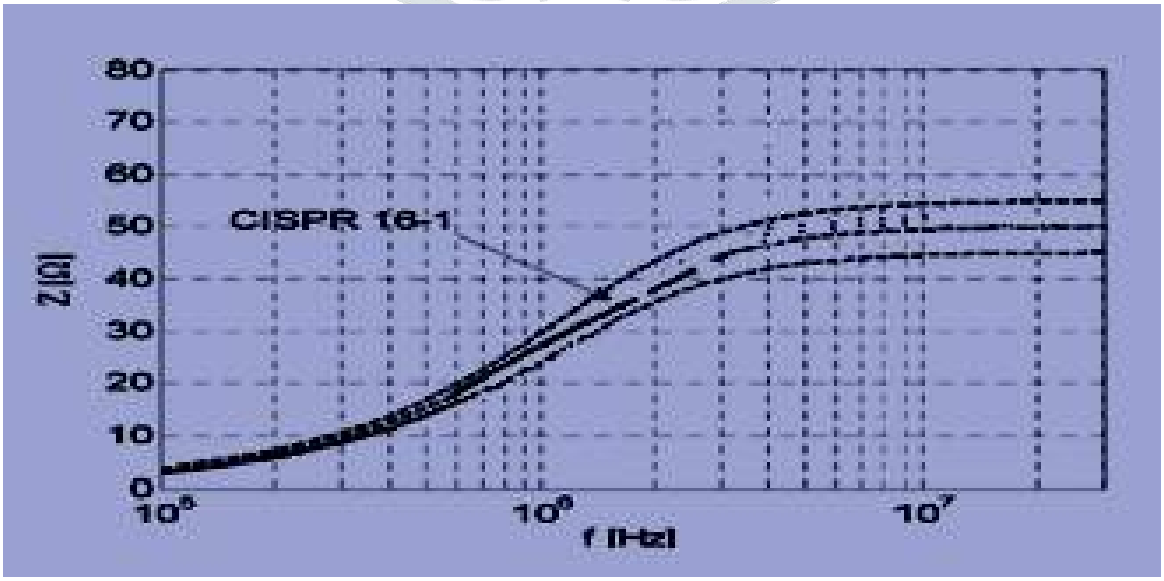


Fig2: Ideal impedance curve of the LSIN as for CISPR16-1

Table 1: specifications of LISN

Topic	Performance Specifications
Frequency	9 KHz – 30 MHz
AMN Impedance	(50 mH + 5 Ω) ‖ 50 Ω
Maximum current	AC / DC 16A
Standard	CISPR 16-1-2
Maximum voltages	AC:250V, 50/60Hz, DC:600V DC
RF Output	50Ω to connect RF output to EMI receiver
EUT Terminal	Output: 3 pin standard socket

III. HIGH FREQUENCY INDUCTION MOTOR MODEL

As a matter of fact, AC drives are more popular because of developments in power electronics in the electrical drives, reduced cost and other maintenance problems. In most of the cases, squirrel cage induction motors are used to avoid inertia and also for easy control of stator in vehicle applications. In this work, 3-Φ, induction motor with rated values of voltage: 415V (±10V), frequency: 50Hz (±5Hz) current: 2.5A, is used for smooth execution.

Similarly for carryout the simulation work the high frequency model of induction motor are designed, which is considered in the literature [1], [18] and several HF models are discussed in [22]. In general common mode currents are measured at the high frequencies only, that's why representation of motor model in high frequency circuit as not at all a problem. High frequency model of an induction motor with simulation values (MATLAB) as shown in fig.5.

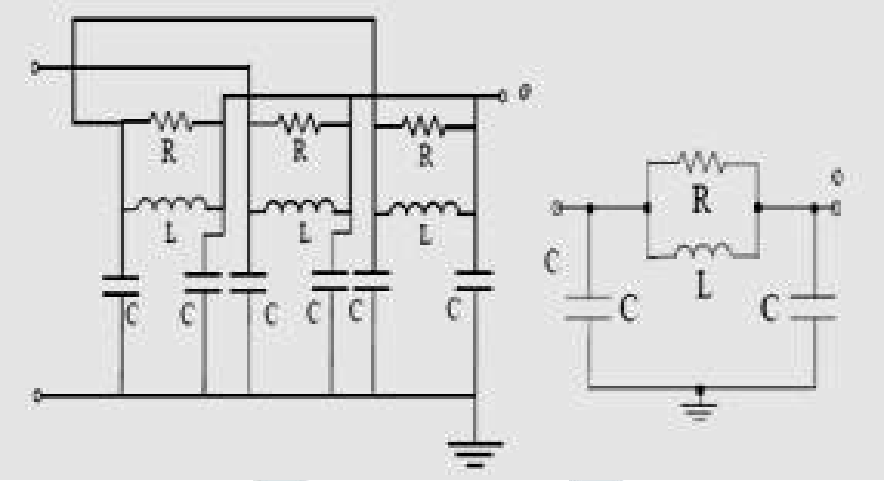


Fig3: High frequency circuit of the induction motor single winding

So many literatures give different values for the motor winding parameters, such as stray capacitances, winding inductances and resistances. Out of all M.C. Di Piazza. Et. al [23] represents more accurate values and she was inspiration for me to motivate towards electric vehicle research area. Those values as given below

Parameter	Value
R	640 Ω
L	1.60 mH
C	899 pF

Table2: Induction motor per phase winding parameters

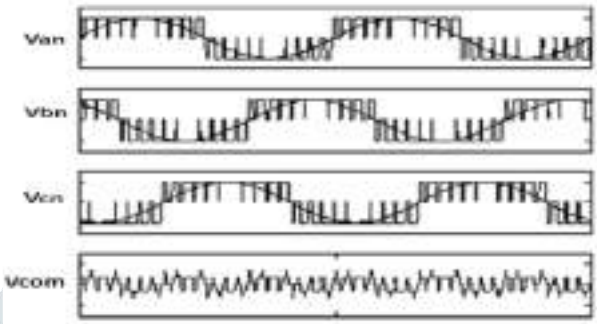
IV. DESIGN OF CMV ACTIVE CANCELLER CIRCUIT

I. Common mode voltage

An average voltage available at neutral point with respect to ground is called as common mode voltage or a voltage that appears in common at both input terminals of a device with respect to the output reference usually ground. Mathematically represents

$$Vm = \frac{[Van+Vbn+Vcn]}{3} \quad (1)$$

In the above equation Van, Vbn and Vcn are the phase voltages generated by the PWM inverter. The waveform of common mode voltage is schematically shown on Figure below. The common mode voltage can be measured between star point of stator winding of an induction motor and the ground.



Generally the common mode analysis without long cable is considered [24], the terminal voltages at the motor would be same as at the inverter output. Therefore common mode voltage

$$Vcm = \frac{Va+Vb+Vc}{3} \quad (2)$$

Where $Va = Va,o + Vo,n$ (3)

$$Vb = Vb,o + Vo,n \quad (4)$$

$$Vc = Vc,o + Vo,n \quad (5)$$

Substituting equations (3)-(5 in equation (2), we have

$$Vcm = \frac{Va,o+Vb,o+Vc,o}{3} + Vo,n \quad (6)$$

Summation of inverter output voltage

$$Vcm = \pm \frac{Vd}{6} + (Vo,n) \quad (7)$$

In this project the length of the cable is very small, that's why not considering any calculations regarding with cable. The effects of common mode voltage on induction motor fed by high switching frequency PWM inverter was more severe. This common mode voltage is the major reason to create a shaft voltage, and resulting bearing currents are produced in the system. Therefore premature damage to the both life time as well as the reliability of the motor. To protect the drive from these abnormalities common mode voltage active cancellers are implemented in early stages to protect the motor.

II. Common mode voltage active canceller

As matter of fact, the common mode voltage was the major reason for shaft voltage. Therefore to neutralize this common mode voltage, an active voltage canceller was designed. This is used mainly to remove the common mode voltage. It works in the following steps; initially it detects the common mode voltage from the output of the inverter by three star connected capacitors, and transferred through the push-pull emitter follower in Darlington configuration and reproduced at the primary of the Common mode transformer.

The Design details of the common mode voltage active canceller (CMVAC) as shown in Fig.6. it consisting of star connected capacitors, C reasonable 0 to 10nF are preferable and C^{I}, which is three times of C, DC voltage source and finally the common mode transformer.

According to the [2], the schematic of a feedback voltage-sensing voltage-compensating active filter shown in fig.4, the common mode voltage active filter works

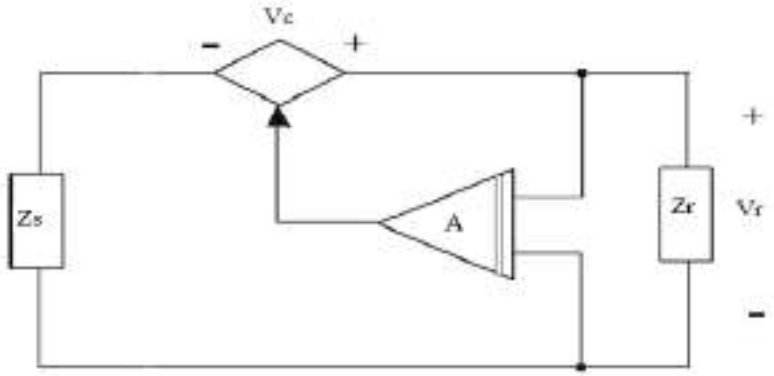


Fig 4: Voltage sensing and voltage compensation

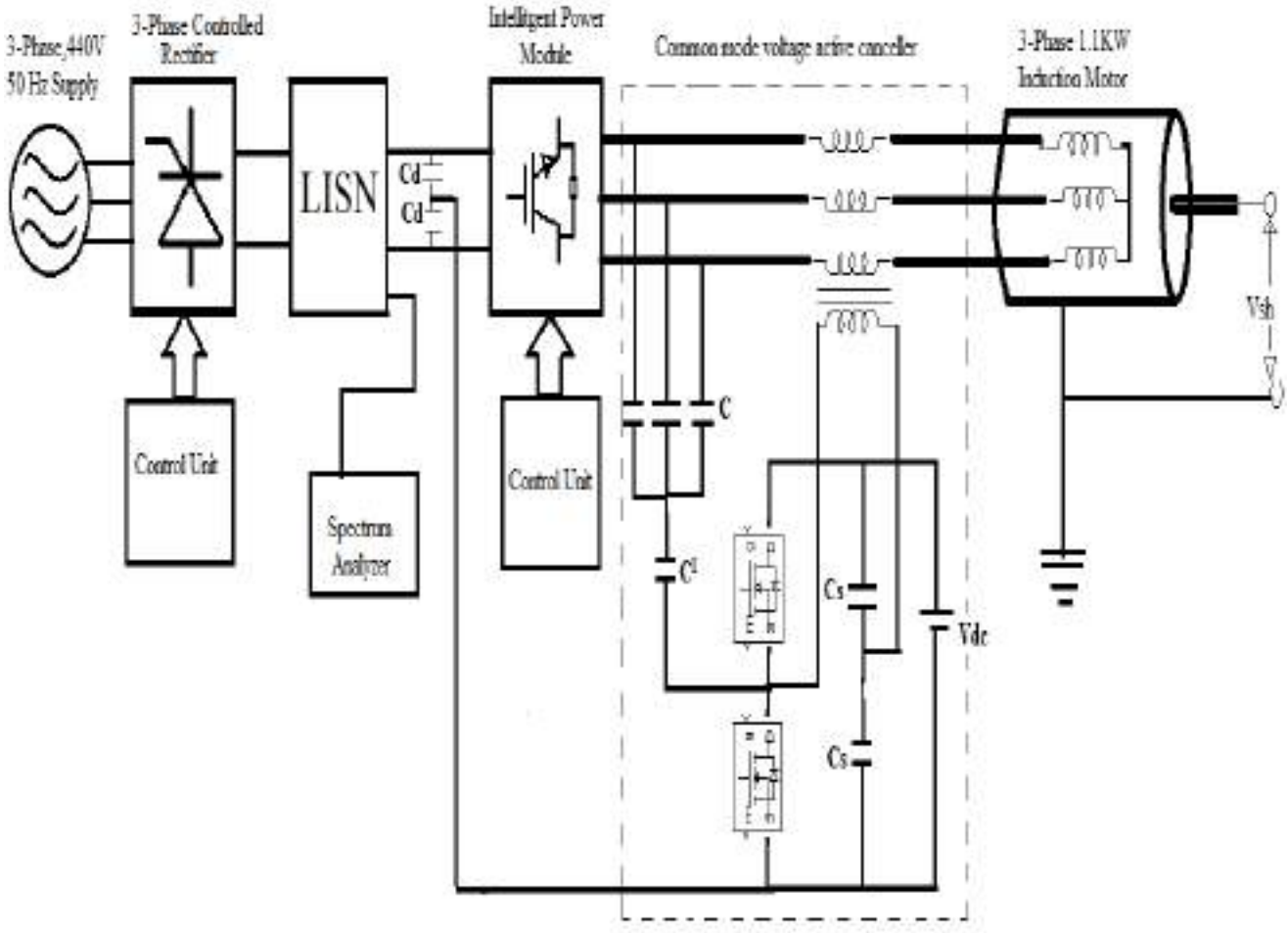


Fig5: An over view of the proposed configuration with common mode voltage active canceller

V. SIMULATION RESULTS

I. Simulated results without filter

For the proposed system in Fig.5 was simulated for both the cases such as without and with active common mode voltage canceller circuits in the MATLAB/SIMULINK as shown in figures. All the results are proposed for without and with filter circuits as shown.

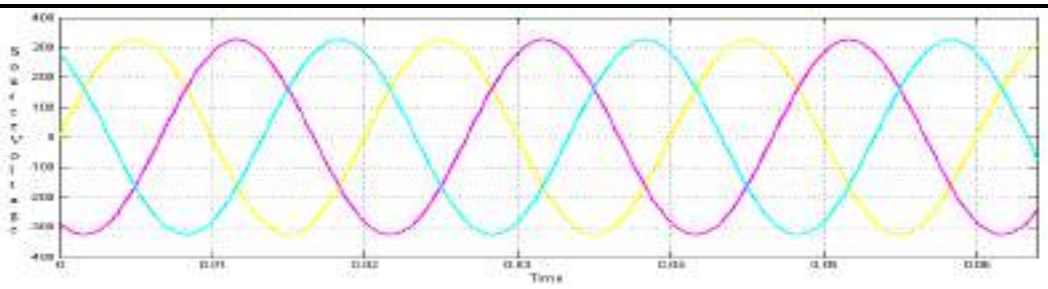


Fig:6 Three phase source voltages

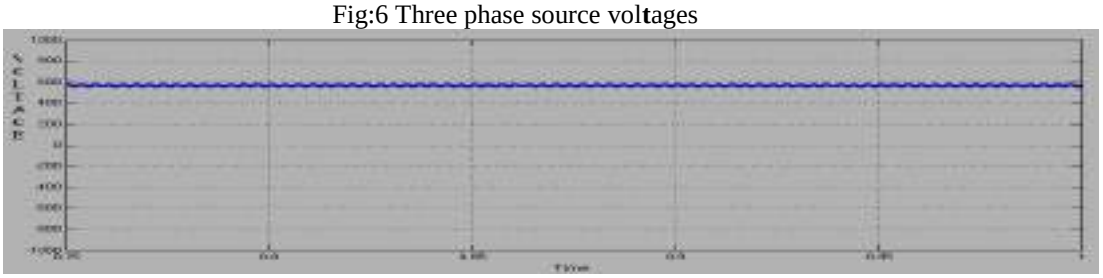


Fig7: 3-phase controlled rectifier output voltage

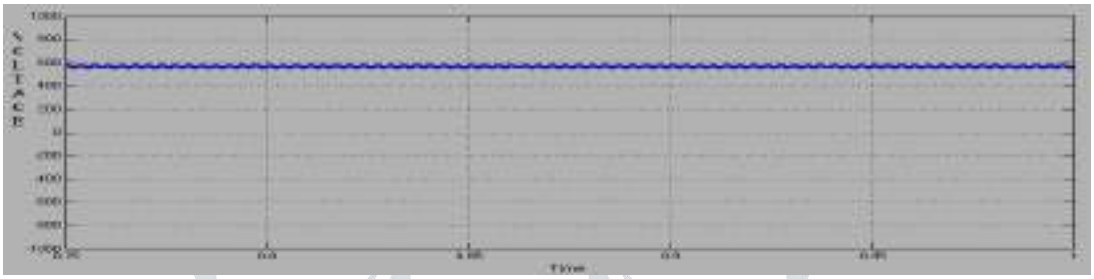


Fig 8: Output of the Line impedance stabilization network

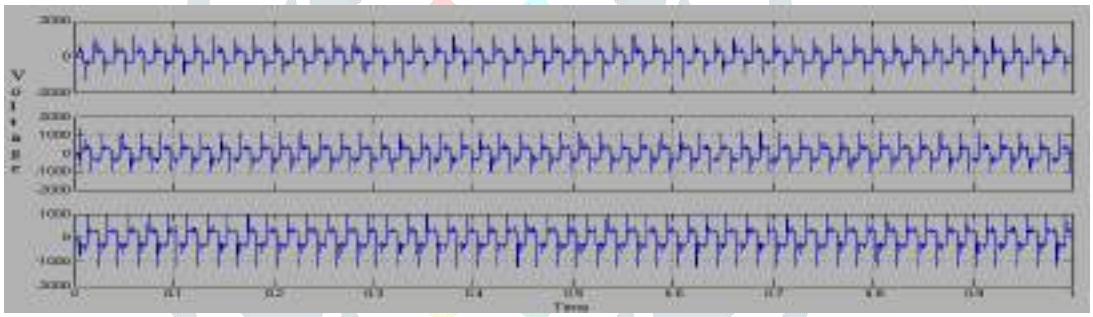


Fig 9: Inverter output voltages of the 3-phases

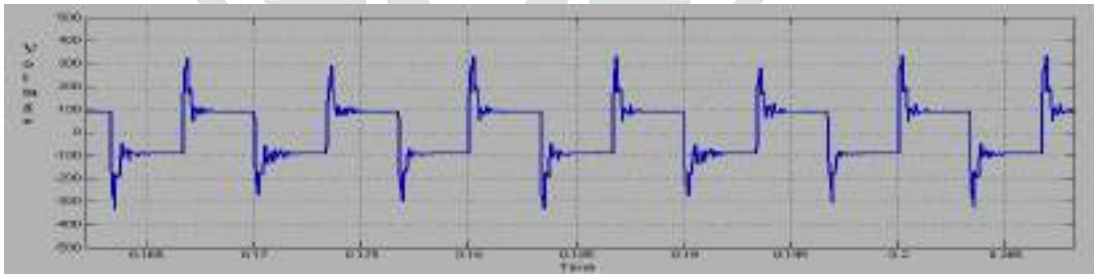


Fig10: Common mode voltage without filter

II. Simulated results with filter

Fig:11 Three phase source voltages

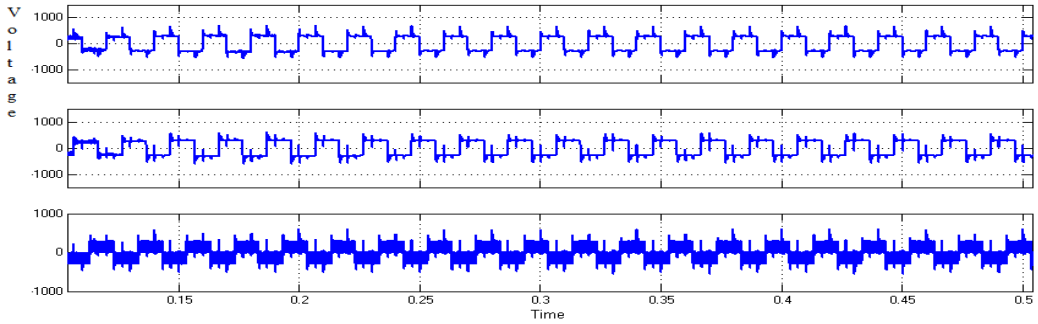


Fig 12: Inverter output voltages of the 3-phases

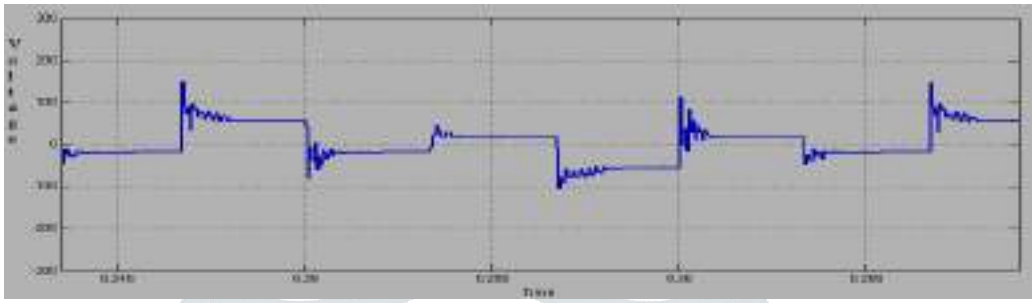


Fig13: Common mode voltage with filter

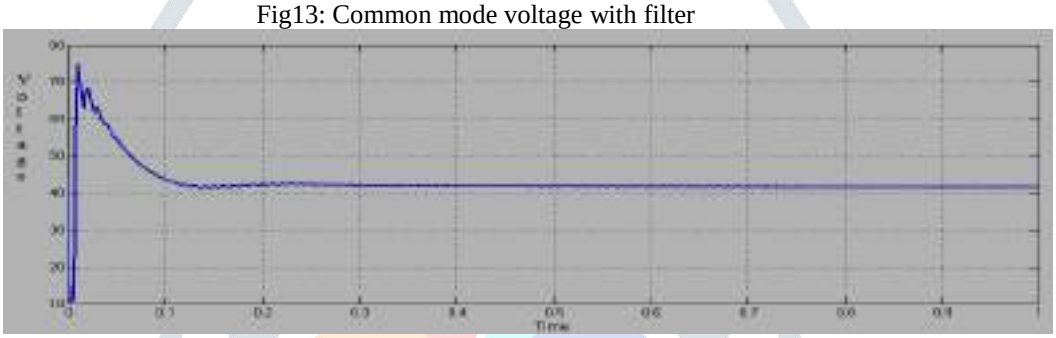


Fig14: Common mode running RMS voltage

VI. CONCLUSION

In this paper, a common mode voltage active canceller (CMVAC) has been developed, which is capable of neutralizing a common-mode voltage generated by high switching frequency PWM inverter. The common mode emissions towards the DC power supply mains are also tested by employing a high voltage dual channel dc LISN designed and build for the simulation purpose. This configuration has been simulated, therefore all the results such as common mode voltage, shaft voltages, common mode EMI those are suppressed satisfactorily. Future scope of the work will execute the prototype common mode voltage active canceller (CMVAC) construction and verify for a 1.1 kW 3-Φ induction motor drive using high switching frequency IGBT inverter.

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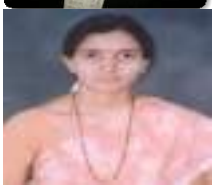

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IMPLEMENTATION OF LMMN-BASED ADAPTIVE FILTERING METHOD FOR CONTROL OF SINGLE-PHASE SOLAR POWER GENERATION SYSTEM WITH UNIVERSAL ACTIVE POWER FILTER

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Abstract
This paper deals with the control of single-phase grid-tied solar photovoltaic (SPV) power generation system with a universal active power filter (UAPF) capabilities. The SPVUAPF system consists of series and shunt voltage source inverters (VSIs). The shunt VSI exports the real power extracted from the PV panels to the grid and local loads. In addition to handling the real power, the shunt VSI provides compensation of reactive and harmonic currents generated by the loads. The reference signals required for the control of the shunt and series VSIs of the SPV-UAPF system are estimated using least mean mixed norm (LMMN) adaptive identification algorithm.

Keywords: Universal Active Power Filter (UAPF), Solar Photovoltaic (SPV), Least Mean Mixed Norm (LMMN).

I. INTRODUCTION

The ever-growing energy demand and emphasis on clean energy have led to proliferation of solar and wind based renewable power generations system. Between solar and wind energy systems, the solar energy systems are widely found at distribution level as they require little or no maintenance and the solar panels can be installed on almost any roof, as well as on the ground. Therefore, many households and commercial places are being powered by solar power [1]. The solar power generating systems make use of power electronics based dc-dc and dc-ac converters to transform the dc voltage generated by the solar panels into a usable ac voltage [2]. The power electronic converters are controlled to operate the solar panels at maximum power point. In case of grid tied solar power generation systems, the voltage source inverters (VSIs) export the remainder of the extracted solar power to the distribution grid upon feeding the local loads. Usually for high power systems, three-phase is preferred as they offer reduced current stress on power electronic switches, improved efficiency, high power density and reduced passive elements size. Nonetheless, single-phase systems are suited for low power generation in the range of a few kilowatts. Most of the rooftop domestic solar power systems are low power and single-phase in nature. In single-phase systems, the number of power electronic switches and sensors required are less compared to a three phase system; which in turn makes the control circuitry simple and cost-effective.

Thereby the complexity of the control system is reduced drastically in single-phase system. However, in case of single-phase systems, the instantaneous powers contain second order oscillations, which would lead to dc-link voltage oscillations in VSIs. To filter out these dc-link voltage oscillations a large capacitor bank is needed on dc side. Lately, the power quality has become a rising concern in distribution systems with the increased use of various nonlinear loads such as variable frequency drives, LED-based lighting devices and switch mode power supplies. The harmonic currents drawn by the nonlinear loads causes harmonic voltage drops in the system and thereby distort the voltage at point of common coupling (PCC). The voltage distortion caused by nonlinear loads may lead to malfunctioning of sensitive loads [3]. The effects of harmonics drawn can be suppressed with the help of power quality conditioning devices such as series and shunt power filters. Installation of dedicated power conditioning devices can be avoided if the VSIs that are employed for the active power generation are able to offer ancillary services like harmonic and reactive currents compensation [4], [5].

II. LITERATURE SURVEY

Various studies focusing on integrating compensation capabilities in the VSIs of grid interactive solar power generation systems can be found in the literature [6]–[12]. Primarily, the attention has given to integration of shunt compensation capabilities like harmonic and reactive currents compensation to improve the voltage quality at the PCC as it does not require any additional component such as a series transformer. In [6]– [8], the solar power generation systems with integrated shunt compensation are reported. However, to deal with the voltage disturbances like voltage sag, swell and harmonic distortion, series compensation [9] is preferred over shunt compensation. Hence, to simultaneously provide both series and shunt compensation, universal active power filters (UAPFs) can be used [13]–[15]. UAPFs are capable of handling most of the power quality problems arise in distribution systems. In [10]–[12], a solar power generation coupled with both UAPF capabilities is proposed.

In the fields of electric drives and power conditioning systems, the least means squares (LMS)-based adaptive technique is being extensively used compared to various adaptive identification methods because of its simplicity and easy to implement. Application of LMS technique for extracting the fundamental frequency component information in a nonlinear load currents reported. Nonetheless, in case of the LMS technique, the mean square error (MSE) is directly related to the step size. The higher the step size, the faster the convergence. However, increasing the step size would lead to increased MSE. Therefore, a judicious value of step size must be selected for extraction of harmonic components. Further, the LMS-based identification technique operates on the principle of minimizing the MSE. Therefore, the LMS method is more suitable when the error norm is below 1.0 and it becomes less responsive when the error norm is greater than 1.0. Another adaptive technique similar to LMS method known as least mean forth (LMF) technique [can also be found in the literature. Unlike LMS method, the LMF technique works effectively when then error is less than 1.0.

Based on the discussion so far, considering the limitations of LMS and LMF techniques, the least mean mixed norm (LMMN) algorithm is identified, modified and applied for adaptive detection of harmonic components of load current and synchronization of single-phase SPVUAPF system in this work. The LMMN method has combined benefits of LMS and LMF techniques. Unlike the reported works, a multi-channel structure of LMMN-based filtering algorithm is proposed for the present application to enable selective compensation and increase the detection speed. The multi-channel LMMN-filter structure simultaneously extracts all the dominant harmonic components of the load current in addition to fundamental to reduce the error to be processed by the LMMN filters and thereby increases the dynamic response of harmonic components detection process.

III. PROPOSED SYSTEM

A. Description of SPV-UPAF System

Fig.1 shows the configuration of single-phase SPV-UAPF system. The system consists of back-back connected single phase H-bridge VSIs labeled as shunt and series inverters with common dc bus. The VSIs are electronically realized using insulated gate bipolar junction transistors (IGBTs). Solar power is extracted from the PV panels by means of a boost converter and fed to grid via shunt VSI. The boost converter operates the solar panels at maximum power point. The switching pulses for the boost converter are generated using perturb and observe (P&O) algorithm. The series VSI is placed between PCC and the load via a single-phase step down transformer. The secondary side voltage of the series transformer either aids or opposes the PCC voltage to regulate the load voltage. The symbols vpcc, vse and vl represent the PCC voltage, series injected voltage and the load voltage, respectively. The quantities ish, ig and il, represent shunt VSI current, grid current, and load current, respectively. The dc quantities such as dc-link voltage, PV output voltage, PV output current are denoted by

Vdc, Vpv and Ipv, respectively.

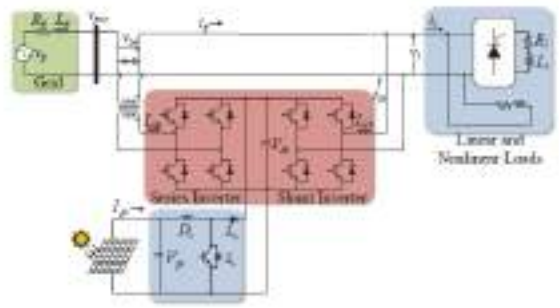


Fig. 1. Schematic diagram of single-phase SPV-UAPF system.

B. Control of SPV-UAPF System

The overall control block diagram of SPV-UAPF system is shown in Fig.2. As one can see, the control of SPVUAPF system requires seven sensors in total out of which three current sensors and four voltage sensors. The detailed diagrams pertaining to the various blocks of the overall control system are shown in Fig.3. The total control of SPV-UAPF is typically into two parts namely series VSI control and shunt VSI control.

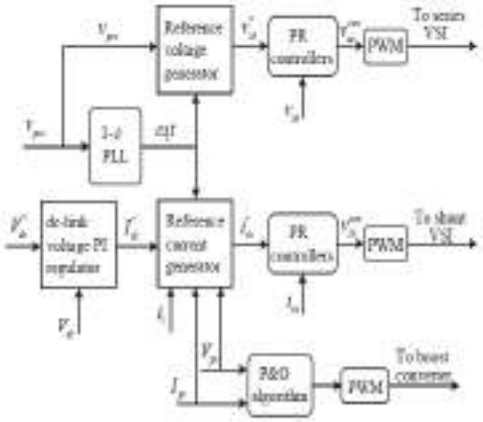


Fig.2. Overall control diagram of single-phase SPV-UAPF system.

C. Series VSI Control

The block diagram illustrating series VSI control is shown in Fig. 3 (a). The series VSI injects a series voltage in-phase or out of phase with the sensed PCC voltage in order to regulate the load voltage. Further, the control system of series VSI should ensure distortion free rated voltage across the load terminals. The reference voltage (v∗ l) to be maintained across the load terminal is estimated as

$$v_l^* = V_{mr} \times \sin \omega_1 t \qquad (1)$$

Where ω1t is phase angle of the fundamental component of vpcc and Vmr is the rated value of peak PCC voltage . The actual PCC voltage (vpcc) is subtracted from the estimated reference load voltage (v_l^*) given in (1) to compute the reference voltage that needs to be injected by the series VSI (v_{se}^*).

$$v_{se}^* = v_l^* - v_{pcc} \qquad (2)$$

The reference voltage of series VSI (v∗ se) estimated by (2) is now compared with its actual voltage (vse) and then the voltage error is processed with a set of proportional-plus resonant controller (PR)

$$v_{se}^{err} = v_{se}^* - v_{se} \qquad (3)$$

The output of PR controllers is added up and then used in sine triangle pulse with modulation for generating gating pulses for the switches of series VSI. The transfer function of a PR controller and its parameter selection for stable operation of the system are reported.

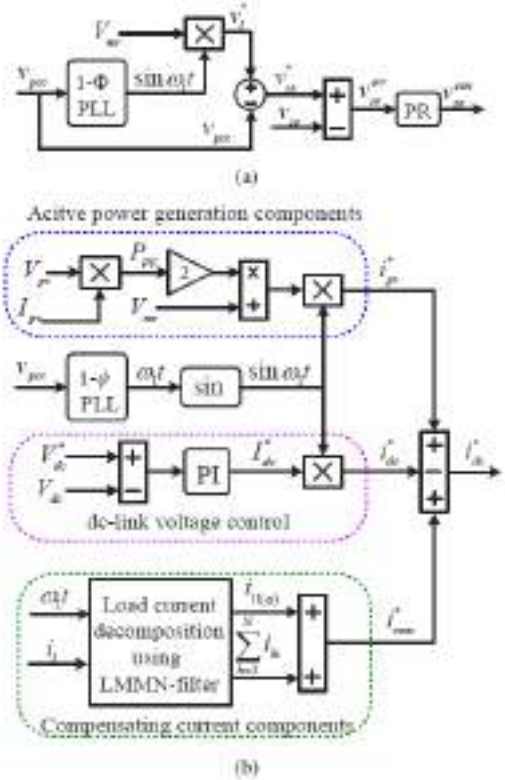


Fig. 3. Detailed block diagram of control scheme for SPV-UAPF system. (a) Series VSI control. (b) Shunt VSI control.

D. Shunt VSI Control

The block diagram of shunt VSI control is illustrated in Fig. 3(b). To simultaneously

handle the active power harnessed from the solar panels and provide mitigation of the harmonic and reactive currents, the shunt VSI is operated in current control mode. Therefore, one has to generate reference currents for the control of shunt VSI. The reference current of the shunt VSI is composed of following three components as illustrated in Fig. 3(b):

1. Active power component.
2. dc-link control component
3. Compensating components.

In the process of estimating compensating components of the reference current signals, the LMMN algorithm is employed. The LMMN filter decomposes the voltage/current signal into fundamental and various harmonic components. Thus the extracted fundamental components are used in reference signals estimation.

IV.SIMULATION RESULTS

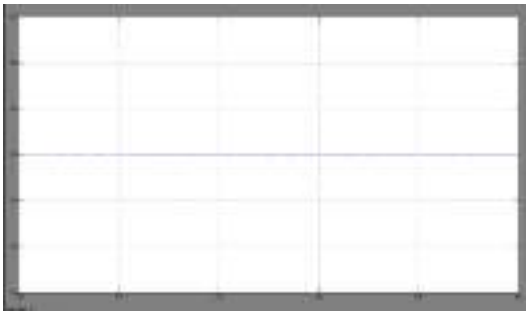
The performance of UAPF-SPV using LMMN-based adaptive filtering algorithm is demonstrated using simulation and experimental studies. Identical operating conditions and system parameters are considered to perform computer simulations and experimental studies. The system parameters are listed in Table 1. The dynamic performance of SPV-UAPF system under various testing conditions such as a step change in solar irradiance, voltage sag/swell and grid voltage distortion is demonstrated and analyzed.

TABLE I
SYSTEM AND CONTROL PARAMETERS

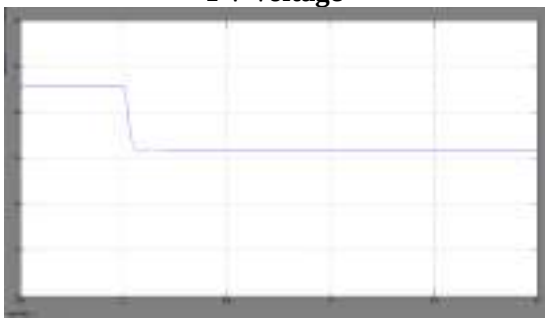
Parameters	Values
Rated PCC voltage (V_{pccr})	240 V
Nominal frequency	50 Hz.
Shunt VSI kVA rating (S_{sh})	13.2 kVA
Shunt VSI filter inductance (L_{sh})	3.0 mH
Series VSI kVA rating (S_{se})	3.0 kVA
Series transformer turns ratio	1:1
Series VSI filter inductance (L_{se})	1.0 mH
PV array data	V_{oc} = 430 V, I_{sc} =24 A, V_{mppt} =350 V, I_{mppt}=22. 5 A, P_{mppt} = 8 kW
dc link voltage	V_{dc} = 400 V
dc link voltage PI controllers' gains	$K_p = 1.3 \times 10^{-3}$, $K_i = 0.28$
Loads	1-ϕ two-pulse rectifier with series connected R_l = 30 Ω and L_l = 300 mH load.
LMMN parameters	$\mu = 2 \times 10^{-5}$ and $\lambda = 0.8$

A. Dynamic Performance of SPV-UAPF System Under Solar Irradiance Variation

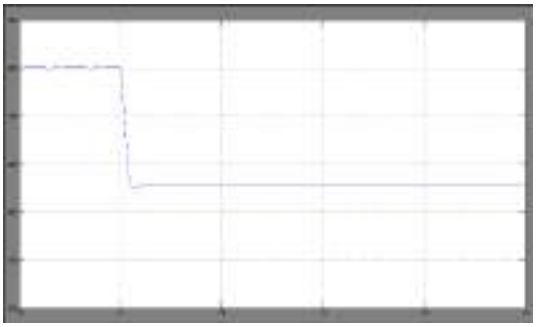
The dynamic performances during a step drop and rise in solar irradiance level are shown in Figs. 4 and 5, respectively. The insolation parameter "G" is the direct indication of solar irradiation. Initially, the solar PV system is being operated at maximum irradiance i.e. 1000 W/m2. As the solar irradiance drops from 1000 to 700 W/m2, the power generated by the PV system reduces. Despite the variation in the PV power generation, the dc link voltage (Vdc) is seen to be well regulated and held constant at its reference value 400 V.



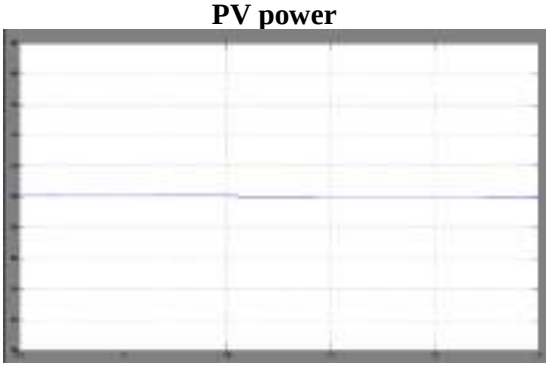
PV voltage



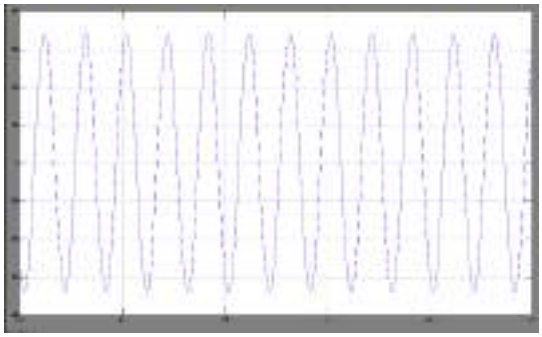
PV current



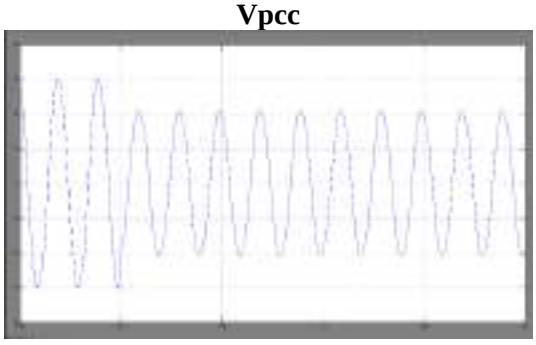
PV power



Vdc



Vpcc



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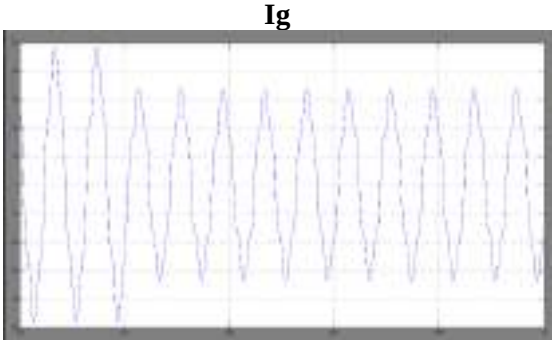

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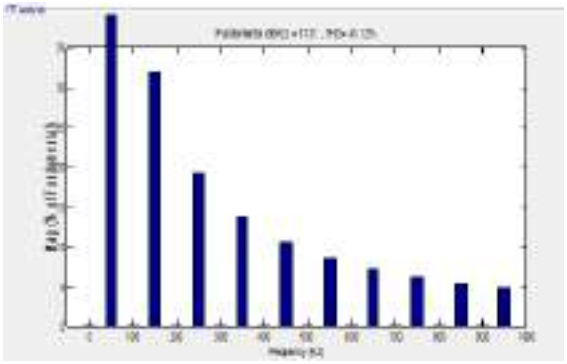
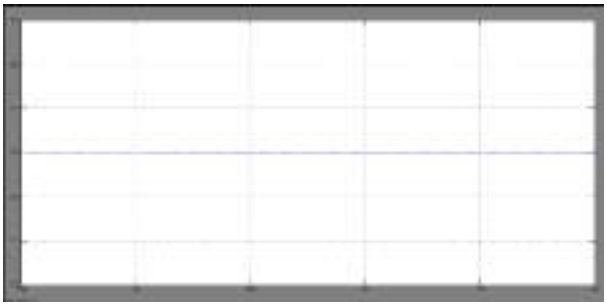
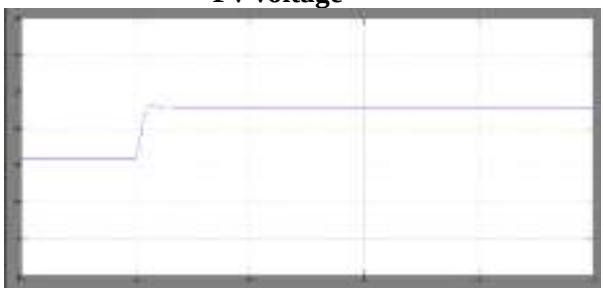


load current THD

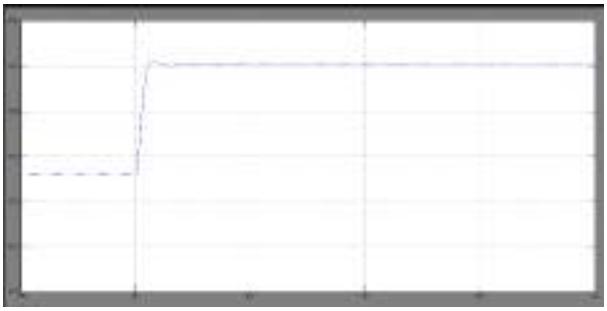
Fig. 4. Performance under a step change in solar irradiance from 1000 to 700 W/m2.



Pv voltage

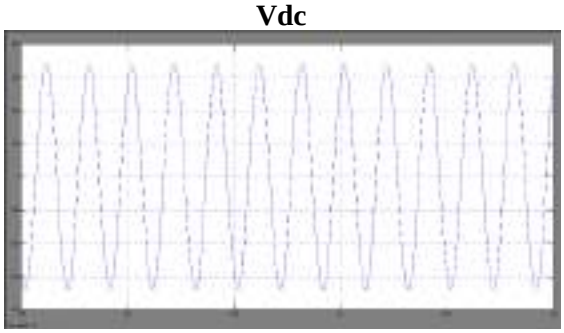


Pv current

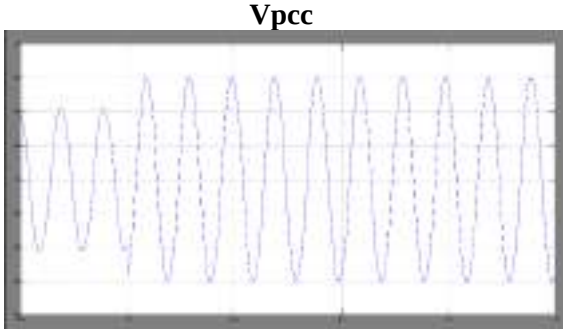


PV power

Vdc



Vpcc



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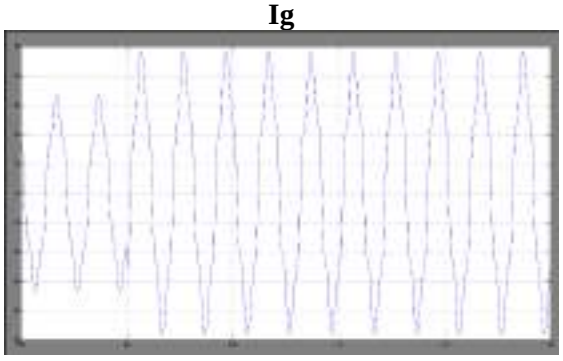

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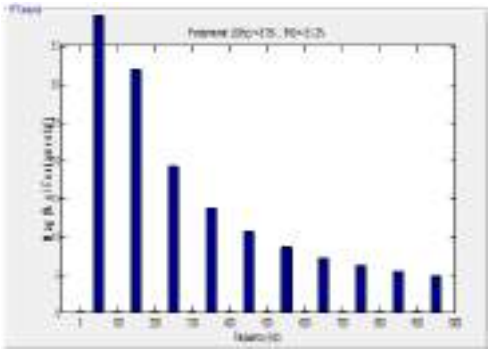
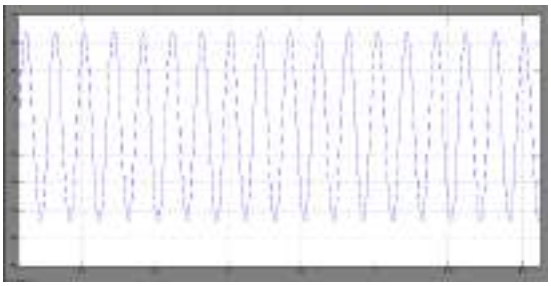


Load current THD

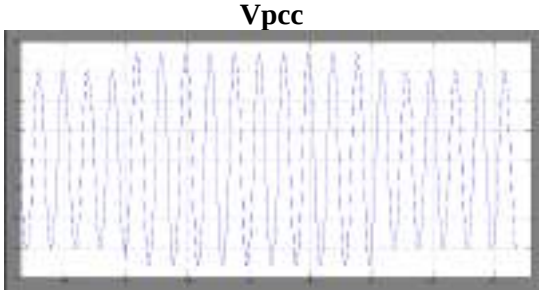
Fig. 5. Performance under a step change in solar irradiance from 700 to 1000 W/m2.

B. Dynamic Performance of SPV-UAPF System Under Load Change

The performance of SPV-UAPF system under load change is depicted in Fig. 6. Simulation results corresponding to load drop and rise are shown in Fig. 6.3, the load on the system is dropped off at t = 0.5 s and the load current il amplitude reduces to half. With the load reduction, the net power being fed in to the grid increases. The performance of the SPV-UAPF system when the load is applied back can be seen from Fig. 6.3. As the load is applied back at t = 0.7 s, il increases and the current ig decreases.



Vpcc



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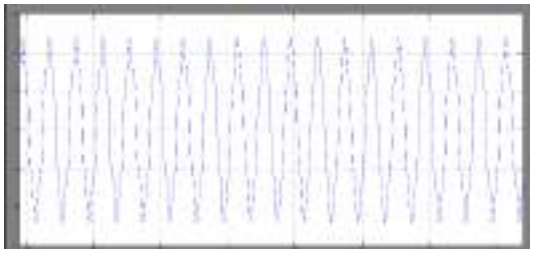

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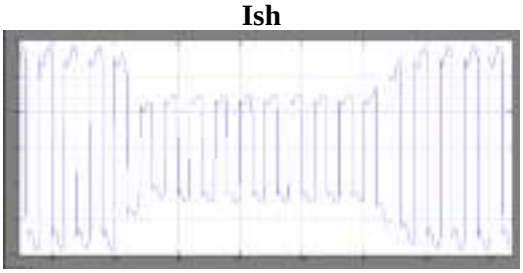

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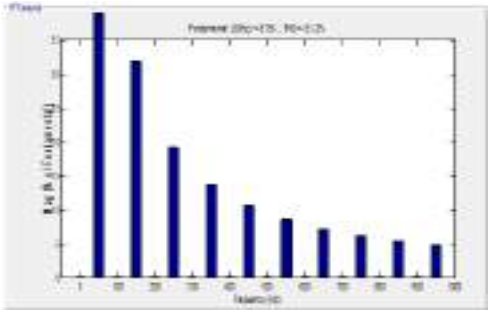
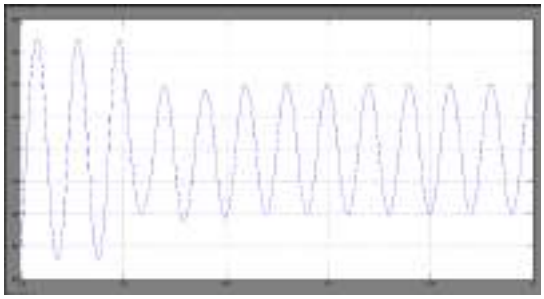


Load current THD

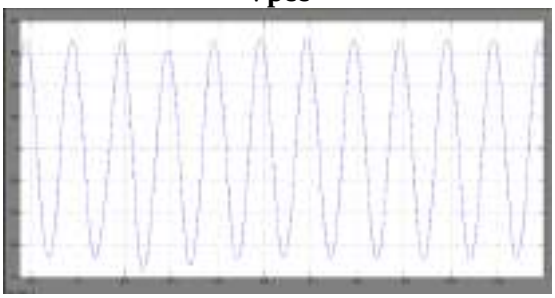
Fig. 6. Performance under a step change in load.

C. Dynamic Performance of SPV-UAPF System Under Voltage Sag and Swell Conditions

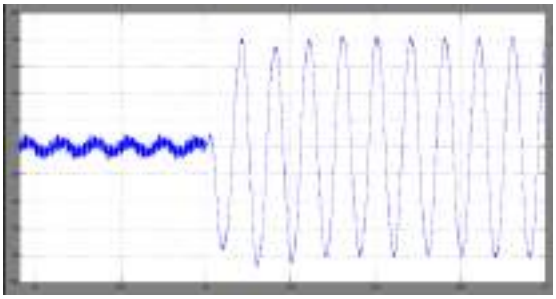
The simulation results corresponding to the performance of the SPV-UAPF system under voltage sag condition are shown in Fig. 7 respectively. The load and PV generations are kept at their peak values. During the voltage sag, the PCC voltage (vpcc) is reduced to 0.7 p.u. The dynamics in the PCC voltage are obtained by varying the grid voltage with the help of a programmable ac source. Similarly, the performance of SPVUAPF system under voltage swell condition can be understood from the simulation results shown in Fig. 8 respectively. As the PCC voltage increases, the series VSI injects vse which is out-of-phase with the PCC voltage.



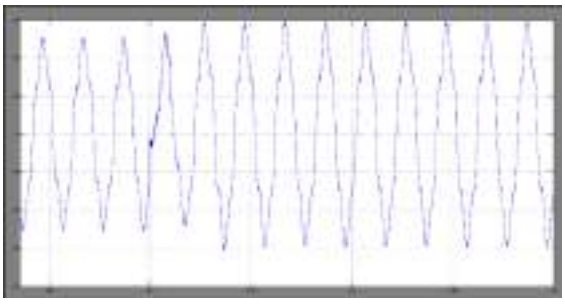
Vpcc



Vl



Vse



Ish

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Fig. 7. Performance under a step change in PCC voltage and Voltage sag.

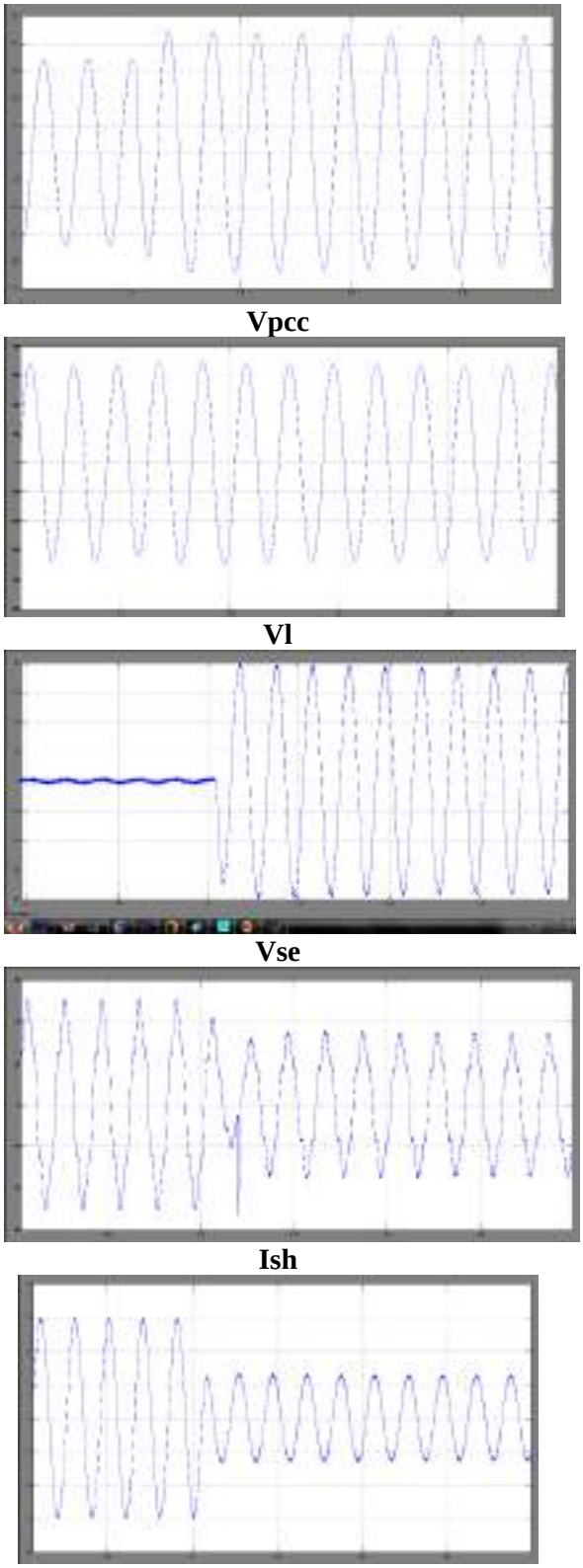
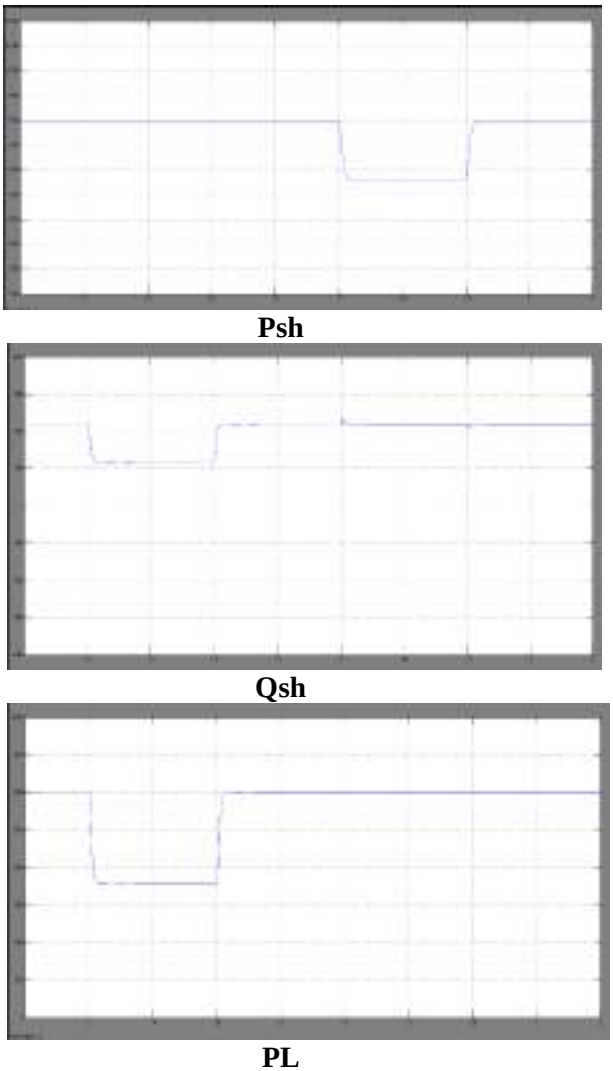


Fig. 8. Performance under a step change in PCC voltage and Voltage swell

D. Variation of Active and Reactive Powers Under Load and Solar Irradiance

The behaviour of active and reactive powers measured across various components of the SPV-UAPF system under a step change in the load and solar irradiance are shown in Fig. 9. For t < 1.3 s, the load is drawing 3 kW of real power (Pl) and 1 kVAr of reactive power (Ql). At the same time, the PV system generated power (Ppv) and maximum powers (Pmpp) are found to be 8 kW, approximately. As the PV power generation is kept constant during the load change, the powers Psh, Pmpp and Ppv are seen to be constant during the load change. After the load change, variation of active and reactive powers during the solar irradiance change with fixed load can also be observed from Fig. 9. At t = 1.7 s, the solar irradiance is reduced from 1000 W/m2 to 700 W/m2. Therefore, the Pmpp and Ppv are reduced and hence the powers Psh and Pg are also decreased. At t = 1.9s, the solar irradiance is increased to 1000 W/m2. Therefore, the powers Psh, Pmpp and Ppv are increased to 8kW.



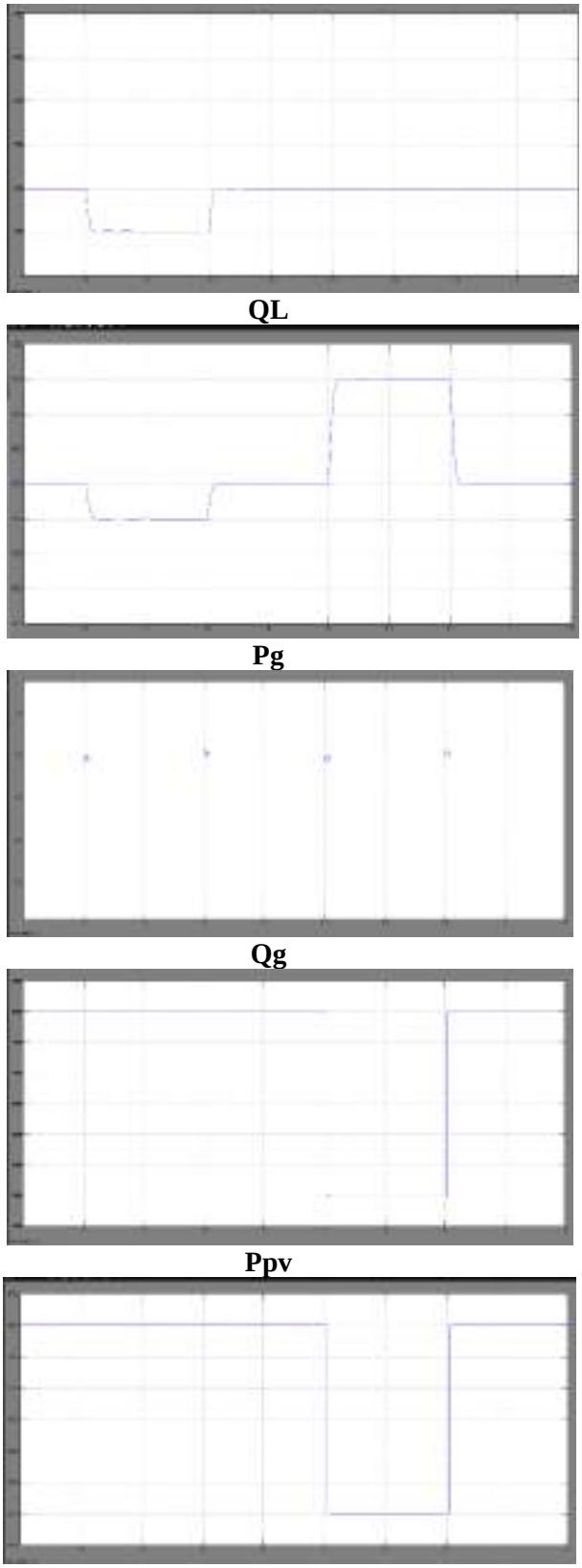
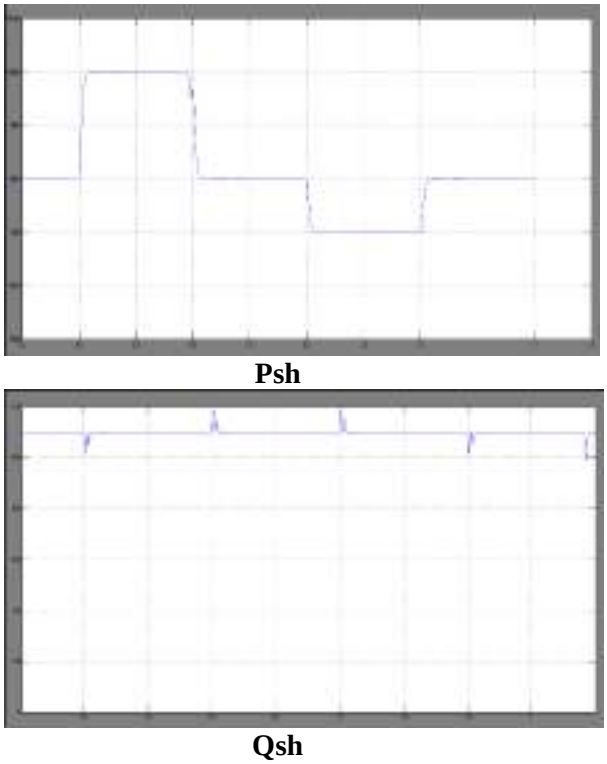
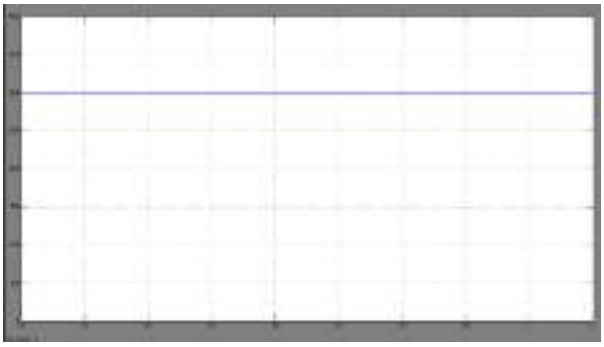


Fig. 9. Active and reactive powers under load and solar irradiance changes

E. Variation of Active and Reactive Powers Under Voltage Sag and Swell

Variation of active and reactive powers during voltage sag and swell conditions are illustrated by Fig. 10. The behaviour under voltage sag is depicted first followed by voltage swell condition. As it can be seen, the voltage sag occurs at t = 0.3s, where the PCC voltage is dropped to 0.7 p.u. Before the voltage sag, Pse is seen zero. As the PCC voltage reduces, the series VSI draws active power to compensate and hence the Pse increases. Despite the voltage sag and swells, the net active power fed into the grid which is the difference between consumed power and generated power is constant. Therefore, the grid power Pg is seen to be constant irrespective of sag/swell. Hence, the compensating reactive power Qsh supplied by the shunt VSI is unchanged which in turn made the grid reactive power $Qg = Ql - Qsh$ unchanged. Further, the series VSI reactive power Qse shown to be zero as it does not contribute to reactive power compensation.





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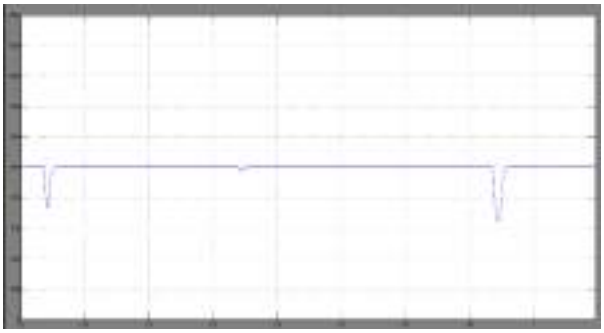

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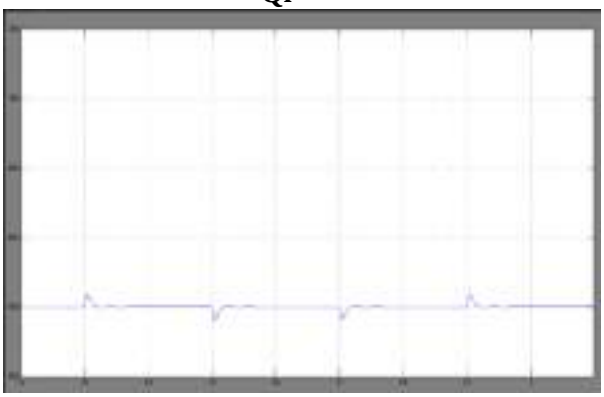

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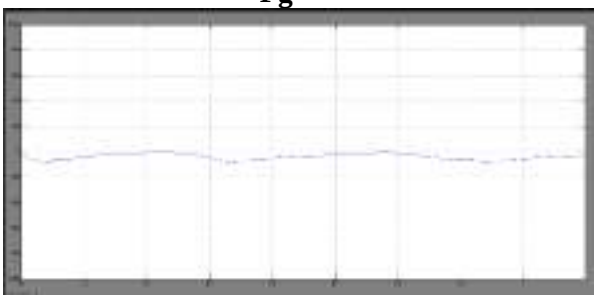

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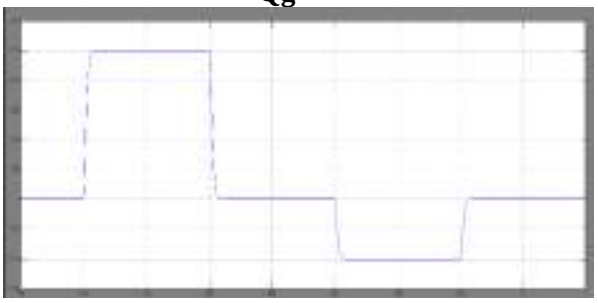

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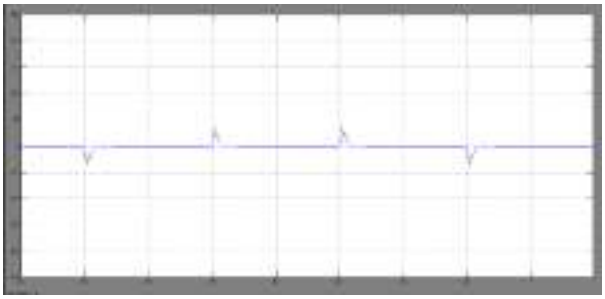

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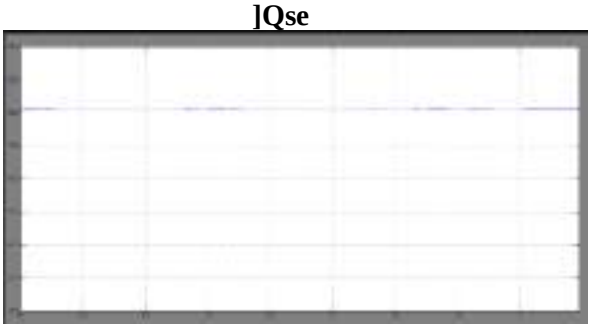
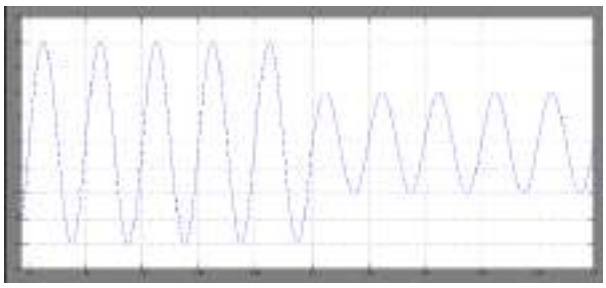


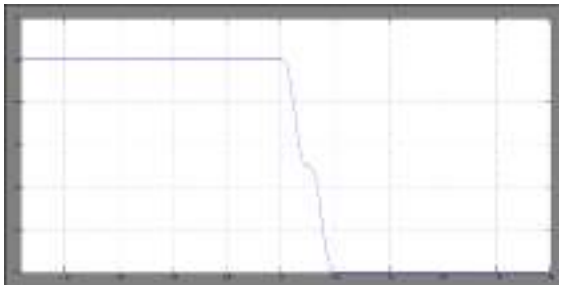
Ppv

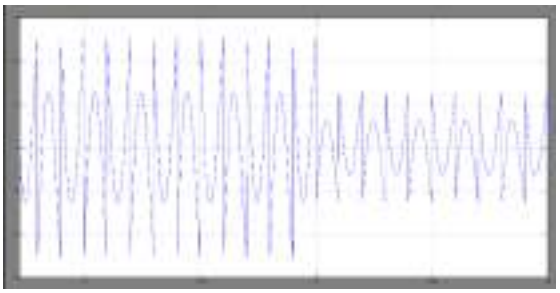
Fig. 10. Active and reactive powers under voltage sag and swell.

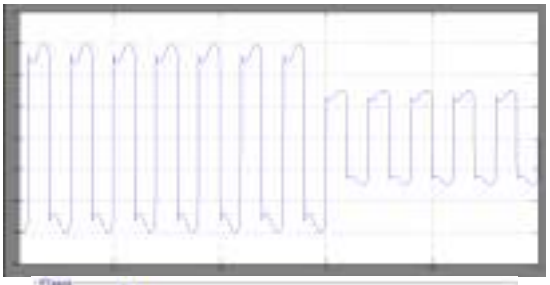
F. PERFORMANCE COMPARISON

The performance comparison is shown in Fig. 11&12 where in the proposed multi-channel LMMN filters-based method is compared against the conventional (synchronously rotating dq frame) method and the recently published adaptive linear neuron ADALINE and the LMF methods. The performances are compared during a step change in the load current il. In addition to il waveform, the waveforms of fundamental load current component il1 and the reference compensation current i∗com estimated by the proposed multichannel LMMN filters-based method, the conventional d-q frame method, ADALINE method and LMF method are shown in Fig. 11&12.









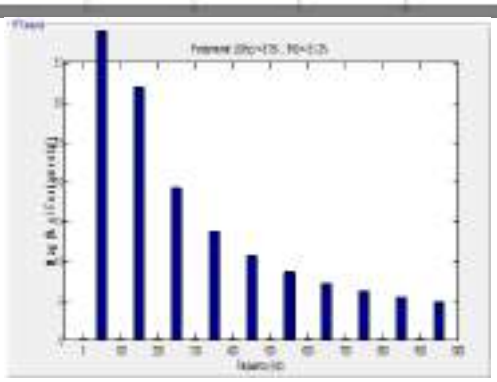
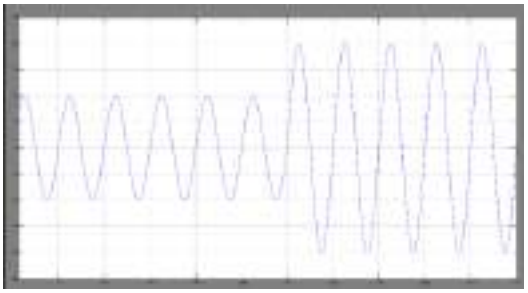
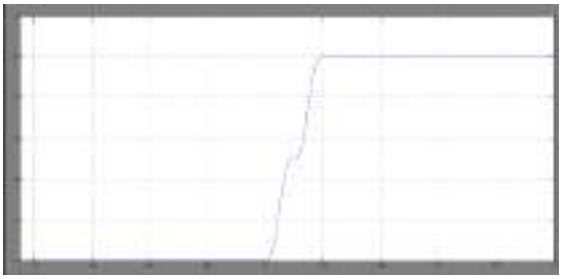
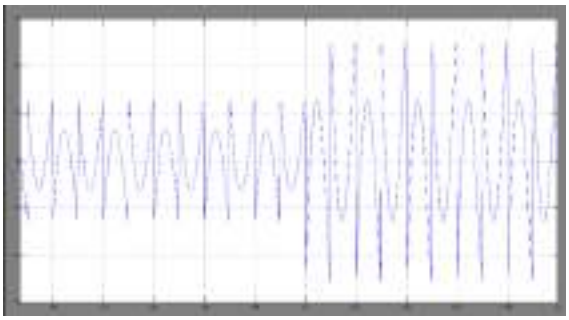
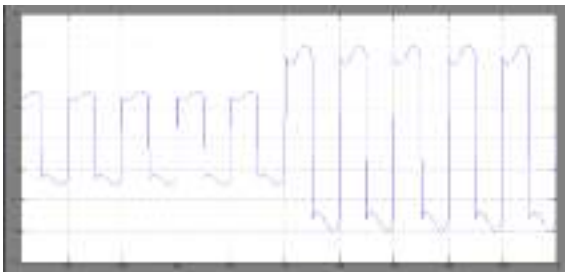


Fig. 11. Performance comparison during load removal









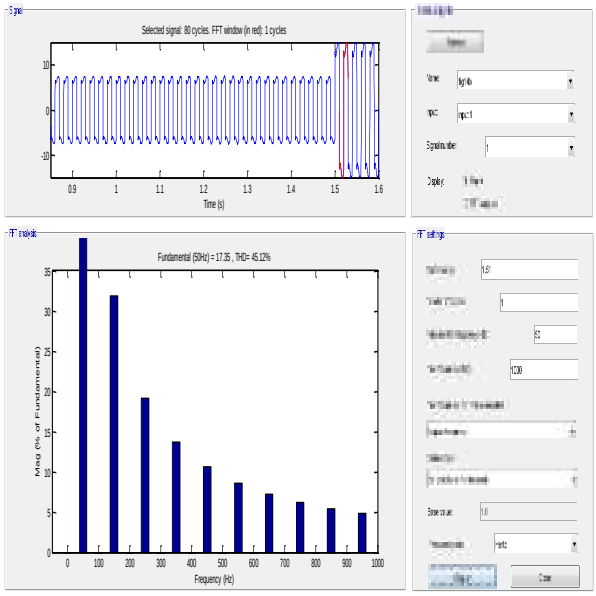


Fig. 12. Performance comparison during load application

V. CONCLUSION

In this paper, a single-phase solar power generation system with integrated UAPF capabilities is designed and its performance using LMMN-based control algorithm is demonstrated. The PCC voltage and load current signals are effectively processed using

multi-channel LMMN algorithm-based adaptive filter to estimate the compensating signal for shunt and series VSIs. Based on the simulation and experimental studies, it is evident that the SPV-UAPF system is able to successfully provide series-shunt compensation and load voltage regulation while simultaneously feeding the power extracted from the PV panels to the grid. The simulation results presented in the paper are shown to be in good agreement. The performance of the proposed LMMN-based control is compared with the conventional and reported methods to demonstrate its superiority in harmonic and reactive currents estimation. Despite the sudden and abrupt change in PCC voltage, the proposed control algorithm could effectively regulate the load voltage magnitude. Further, the THDs of grid current and load voltage are well maintained below 5%.

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Case Study JoALS

Engineering College Websites in Andhra Pradesh: An Evaluation Study

O. Seshaiah[1,*], R.V. Rekha[2], Ch. Veeranjaneyulu[3]

Abstract

The academic institutions in Andhra Pradesh have begun to recognize the importance and potential of using the World Wide Web. Since the early 1990s, colleges have started designing websites and offering services on the internet. The web pages of colleges have many designs and varieties, but it is necessary for these websites to follow a certain framework in their design based on their users, which increases the need for the evaluation of these websites. In reality the goal behind the evaluation of college websites is to guide them toward providing the users with accurate, correct, and authentic information. The goal of this study is evaluation of the engineering college websites in Andhra Pradesh to assess user's opinion. A questionnaire survey was conducted among the top 20 engineering colleges which were identified through the website evaluation checklist.

Keywords: Academic websites, Andhra Pradesh, engineering colleges, website evaluation, web credibility, web usability

INTRODUCTION

Web technology is one of the most important and complex inventions of mankind. It is a powerful means of communication, dissemination, and retrieval of information. The academic institutions in Andhra Pradesh have begun to recognize the importance and potential of using the web as a tool to make valuable and up-to-date information available to user community.

Since the early 1990s, colleges have started designing websites and providing services via the internet. Today, the amount of information published on the internet, in particular information on the World Wide Web is considerably higher than that on other media. College web pages have many designs and varieties, but there is a need for a framework in their user-based design, which increases the need for evaluation of these websites [1]. Because college websites play an important role in providing the required services to users, suitable methods for evaluating these sites are of great importance. In reality the goal behind the evaluation of college websites is to guide them toward providing the users with accurate, correct, and authentic information. The purpose of this study is the evaluation of the engineering college websites of Andhra Pradesh on the basis of a questionnaire.

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Engineering Education in Andhra Pradesh

Technical education in Andhra Pradesh has seen tremendous growth over the past two decades, both in the number of students and faculty. The recent growth in the Andhra Pradesh technical education is overwhelming because educational institutions

with private funding came forward to establish technical institutes rather than educational institutions with public funding.

New Andhra Pradesh was formed as a separate state after bifurcation in 2014. According to the All India Council for Technical Education [2], there are 344 technical institutes or colleges in Andhra Pradesh during the academic year 2014–15. Among them, 10 are public, 331 private and 3 university managed colleges.

Objectives

The main aim of the study is to evaluate the engineering college websites in Andhra Pradesh. The objectives of the study are:

- To examine users opinion on accuracy, currency, accessibility, consistency, usefulness and performance of the top 20 engineering college websites.
- To assess the content organization and navigation features of the websites from the users' point of view.
- To evaluate the engineering college websites with regard to their user support features as per the opinion of the users.

Related Research

Panneerselvam [3] has studied various features available on Tamil Nadu universities' websites and to find information on library services offered by universities. He noted that important services are offered by most university websites. Remote access, plagiarism control, subject gateway, RSS feeds and social networking activities in the library need to be strengthened.

Jayasundari and Jeyshankar [4] investigated the credibility of IIM websites and its library web pages. The home pages of the IIMs website must be logically structured and their library pages periodically evaluated according to criteria such as access, contact information, authority, currency, ease of navigation, and so on. It is also observed that currency statement like last update details, number of visitors, certifications have not been provided in any of the IIMs website.

Khatri and Baheti [5] analyzed the various aspects of the credibility of websites deemed universities of Maharashtra. A study shows that all deemed university websites are different in many ways. The website and pages of the library must be periodically evaluated against established criteria such as website design, accessibility, accommodations, etc. which will help to improve website according to the user's need and credibility and reliability issue.

Kothainayakis [6] tries to identify the credibility factors of academic websites in three districts of Tamil Nadu. The research shows that most university websites are regularly updated, with the exception of arts and sciences and some other websites. All educational sites are easy to use. However, the organization of information varies from domain to another. A lot of attention has been paid to the design of websites.

Sife and Msoffe [7] conducted a study to evaluate the quality of the websites of five selected public universities in Tanzania. It appears that regularly updating websites is also essential to make them effective and to meet the changing needs of users.

Kannappanavar and Biradar [8] studied and analyzed the various aspects of the credibility of the websites of the Dental College in Karnataka. The research shows that all websites of dental schools differ in many respects. The evaluation of the use of websites of universities in Bangladesh is being studied by Islam and Tsuji [9] from usability perspectives. Two online automated tools used along with a questionnaire. The study found that users are not satisfied with the overall level of use of these sites. Some aspects of design, interface and performance have weaknesses.

Haneefa and George [10] conducted a study that would help Indian universities develop strategies and policies that would make better use of internet resources for education and research. Most doctoral students search the internet with the help of simple keywords. Google is the most popular search engine, followed by Yahoo.

Babu et al. [11] analyzed the various aspects of the credibility of university websites in Tamil Nadu. They found that universities had their own websites; they lacked standard design and structure. Mustafa and Al-Zoua'bi [12] in their study evaluated usability of the academic websites of Jordan's Universities. Two online automated tools, namely: html toolbox and web page analyzer were used along with a questionnaire for users of these sites. The results showed that the overall usability level of the studied websites is acceptable.

Hirwade [13] evaluated the websites of Indian universities, paying particular attention to the web pages of their library. Of the 273 universities, 91 have information about their libraries on their websites. Important findings and suggestions were presented and the directory of Indian university websites was created as a by-product of the research.

Tillotson [14] tested students' understanding of the need for website evaluation and their ability to articulate criteria for evaluation by using a questionnaire at two Canadian universities, through which he revealed that students view web sources somewhat critically and are aware of standard website evaluation criteria.

Kapoun [15] has defined five criteria for evaluating websites. Six website evaluation standards proposed by Collins [16] have received a lot of attention in this area, such as "content, authority, currency, organization, search engine and accessibility". Kirk [17] of Johns Hopkins University made few remarkable contributions in developing the standard criteria for evaluating the websites. Kovacs et al. [18] emphasized the need to evaluate information on the internet and advised not to believe everything that had been found, but to look for the author's background and skills.

Nielsen [19] and Rubin [20] pioneered the testing of websites to determine whether met users' needs. They adapted usability-engineering techniques developed for computer software design and applied them to web design. The usability is recognized as an important quality factor of any modern website.

METHODOLOGY

There were 344 engineering colleges spread over the 13 districts of Andhra Pradesh. Out of the 344 engineering colleges, 277 college websites which were functioning during the study period were taken for data collection.

To assess user's opinion on the engineering college websites in Andhra Pradesh, a questionnaire survey was conducted among the top 20 engineering colleges (Appendix) which were identified through the website evaluation checklist. A sample of 1800 students and 200 faculty members are selected from the total population. A total of 2000 questionnaires were distributed among the students and faculty members, out of which 1815 questionnaires were received back and the response rate is 90.75 percent. The data were collected during the period February 2016 to April 2016 by visiting the engineering colleges. The data analysis was carried out with the help of MS-Excel and SPSS. The collected data were analyzed and presented in the form of tables and graph.

ANALYSIS AND DISCUSSION

Demographic Characteristics of the Respondents

Out of 1815 respondents, 91.2 percent are students and 8.8 percent are faculty members. Majority of the respondents under the study consisted of male from both the students and teaching fraternity.

Among the 1815 respondents, large number of respondents (24.2 percent) are in the CSE Department, it is followed successively by ECE (23.2 percent), EEE (22.3 percent), ME (16.7 percent), Civil (7.1 percent), IT (5.4 percent), Chemical (1.0 percent). It can be observed that the majority of respondents from CSE Department.

Use of the Website

The importance of general feature i.e., use of the college websites was obtained based on a five point scale i.e., very difficult, difficult, no opinion, easy and very easy. The percentage is calculated based on the opinion given by respondents and shown in Table 1.

Table 1 reveals that nearly half of the respondents rated use of website as difficult. It also found that almost fifty percent of the students (49.9 percent) and faculty members rated use of website as difficult and nearly half of faculty members (49.7 percent) also rated use of website as easy. The analysis showed that the p-value is less than 0.01. It is concluded that there is significant difference between students and faculty members in their opinion with regard to the use of website.

Speed of the Website

The site of any institute or organization should be constructed in such a way that it should be accessed within seconds. If a site is taking more time to appear on the screen, it no longer attracts the user. The percentage calculated based on their opinion was shown in Table 2.

Table 2 reveals that more than half of the respondents (55.2 percent) of the college websites opined that speed of website is slow. Very less percentage of students (4.4 percent) rated the speed of website as high. It is also evident that there is a significant difference between students and faculty members in their opinion with regard to speed of website. It is indicated by the Chi-square value, which is significant at 0.01 level with 4 degrees of freedom. A similar study done by Shivabasappa [21] on library websites of R&D institutes of India which reveals that most of the users have rated their websites as very good and excellent for loading speed.

Table 1. Use of the website.

Use of Website	**Category**			**Chi-Square Value**	**p-value**
	Students	*Faculty Members*	*Total*		
Very Difficult	114 (6.9%)	3 (1.9%)	117 (6.4%)	25.703**	0.000
Difficult	827 (49.9%)	76 (47.8%)	903 (49.8%)		
No Opinion	45 (2.7%)	-	45 (2.5%)		
Easy	578 (34.9%)	79 (49.7%)	657 (36.2%)		
Very Easy	92 (5.6%)	1 (0.6%)	93 (5.1%)		
Total	1656 (91.2%)	159 (8.8%)	1815 (100.0%)		

***significant at 0.01 level.*

Table 2. Speed of the website.

Website Speed	**Category**			**Chi-Squire value**	**p-value**
	Students	*Faculty Members*	*Total*		
Very slow	363 (21.9%)	19 (11.9%)	382 (21.0%)	57.839**	0.000
Slow	911 (55.0%)	91 (57.2%)	1002 (55.2%)		
No Opinion	95 (5.7%)	-	95 (5.2%)		
Quick	208 (12.6%)	49 (30.8%)	257 (14.2%)		
High Speed	79 (4.8%)	-	79 (4.4%)		
Total	1656 (91.2%)	159 (8.8%)	1815 (100.0%)		

***significant at 0.01 level.*

Browser Compatibility

It is very much clear from the study that students as well as faculty members opined that none of the college websites was suggested with browser compatibility. Similar results were also reported in the research work carried out by Babu et al. [11] which supported the results of the present study. Their study reveals that many do not provide information about the browser compatibility.

Content Organization

The users were asked various aspects of content organization of websites namely design and sequence of pages, language and terminology, adequacy and organization of content, accessibility and linking to other websites on five point scale. The responses are shown in diagrammatically in Figure 1.

Figure 1 reveals that nearly half of the respondents (48.3 percent) did not express any opinion about design of individual pages. More than half of the respondents (51.9 percent) rated fair about content of the website meeting user expectations. Nearly one-third of them rated it as good. Nearly half of the respondents (48.5 percent) did not express any opinion about language and terminology of website.

Nearly half of the respondents (48.9 percent) rated organization of information on their websites as fair. Nearly one-fourth of the students rated it as good.The results of the present study substantiated results of the study conducted by Kothainayaki [6] which revealed that more than four-fifths of the academic websites have simple organization of information and easy retrieval.

Nearly half of the respondents (46.7 percent) rated sequence of the pages as fair. Over a one-fifth of them rated it as good. The similar results were also reported in the research work carried out by Kothainayaki [6] which revealed that sequencing of information in more than four-fifth of the academic websites is simple and easy to understand by the users. More than two-fifth of respondents did not express any opinion about access required information in minimum click. More than half of the respondents rated links to other related sources as fair. There is significant difference between students and faculty members in their opinions with regard to content organization. It may be faculty members more aware about website.

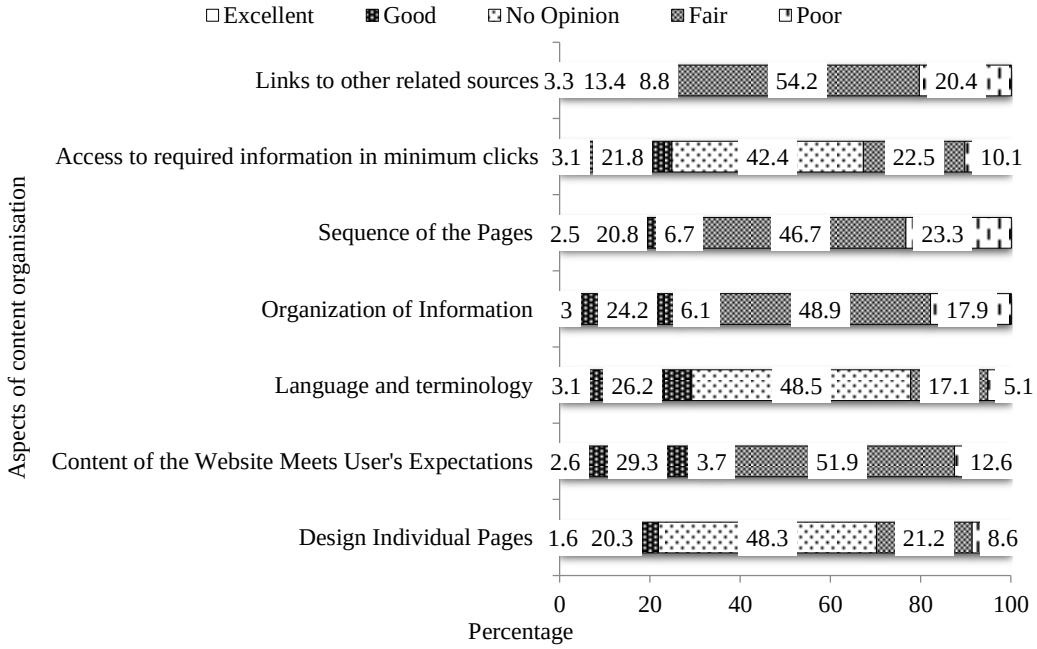

Figure 1. Content organization.

Performance Effectiveness

The users were asked various aspects of performance effectiveness of the websites. The percentage is calculated based on the opinions given by the users and the same is given in Table 3.

Table 3 reveals that more than two-fifth of respondents (44.9 percent) did not express any opinion about less time to download a file or open a page. Nearly one-fifth of them rated it as good. With respect to distinguish between visited and nonvisited links, it reveals that 42.4 percent of the users rated it as fair. 43.2 percent of students rated it as fair whereas 34 percent of faculty members rated it as fair. More than two-fifth of respondents (42.2 percent) rated as fair about information is up-to-date. Over a two-fifths of respondents (44.6 percent) rated as fair about website attract user attention/interest. A meagre percentage of them rated it as excellent (2.5 percent).

Nearly half of the respondents rated as fair about attractive interface design. More than one-fifth of them rated it as good. A good number of students and majority of the faculty members rated the attractive interface design of the website as fair. Over a half of the respondents (51.8 percent) rated view of website as fair. Nearly one-fourth of the students (24.2 percent) rated it as good whereas nearly two-fifths of the faculty members (39.6 percent) rated it as good. Nearly half of the respondents (47.2 percent) rated use of multimedia in college websites as fair.

The t-test values show that there is a significant difference between students and faculty members in their opinions with regard to performance effectiveness.

Navigation Features

Consistent navigation makes it easy to use a website. The navigation features of the websites are analyzed based on opinions of the respondents. The percentage was calculated and same is given in Table 4.

Table 3. Performance effectiveness.

Description	**Students (n=1656)**					**Faculty Members (n=159)**					**Total (*n*=1815)**					**t-value**
	Ex	*G*	*NO*	*F*	*P*	*Ex*	*G*	*NO*	*F*	*P*	*Ex*	*G*	*NO*	*F*	*P*	
1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*
Less time to download a file or open a page	40 (2.4)	268 (16.2)	730 (44.1)	338 (20.4)	280 (16.9)	3 (1.9)	35 (22.0)	85 (53.5)	30 (18.9)	6 (3.8)	43 (2.4)	303 (16.7)	815 (44.9)	368 (20.3)	286 (15.8)	3.034* (0.019)
Distinguish between visited and not visited links	89 (5.4)	277 (16.7)	167 (10.1)	715 (43.2)	408 (24.6)	18 (11.3)	45 (28.3)	5 (3.1)	54 (34.0)	37 (23.3)	107 (5.9)	322 (17.7)	172 (9.5)	769 (42.4)	445 (24.5)	2.902* (0.022)
Information is up-to-date	38 (2.3)	402 (24.3)	188 (11.4)	697 (42.1)	331 (20.0)	1 (.6)	56 (35.2)	8 (5.0)	73 (45.9)	21 (13.2)	39 (2.1)	458 (25.2)	196 (10.8)	770 (42.4)	352 (19.4)	3.055* (0.018)
Website attracts user attention/interest	43 (2.6)	320 (19.3)	150 (9.1)	736 (44.4)	407 (24.6)	3 (1.9)	44 (27.7)	2 (1.3)	74 (46.5)	36 (22.6)	46 (2.5)	364 (20.1)	152 (8.4)	810 (44.6)	443 (24.4)	2.799* (0.024)
Site interface design	55 (3.3)	346 (20.9)	134 (8.1)	796 (48.1)	325 (19.6)	2 (1.3)	52 (32.7)	2 (1.3)	82 (51.6)	21 (13.2)	57 (3.1)	398 (21.9)	136 (7.5)	878 (48.4)	346 (19.1)	2.614* (0.030)
View of website	34 (2.1)	400 (24.2)	97 (5.9)	864 (52.2)	261 (15.8)	2 (1.3)	63 (39.6)	4 (2.5)	76 (47.8)	14 (8.8)	36 (2.0)	463 (25.5)	101 (5.6)	940 (51.8)	275 (15.2)	2.233* (0.045)
Multimedia usage	65 (3.9)	344 (20.8)	165 (10.0)	794 (47.9)	288 (17.4)	9 (5.7)	45 (28.3)	11 (6.9)	63 (39.6)	31 (19.5)	74 (4.1)	389 (21.4)	176 (9.7)	857 (47.2)	319 (17.6)	2.576* (0.031)

Note: 1. Ex: Excellent; G: Good; NO: No Opinion; F: Fair; P: Poor;

2. Col.2–Col.16: Figures in parentheses indicate percentage; Col 17: Figures in parentheses indicates probability values;

*3. *significant at 5 percent level df=4.*

Table 4. Navigation features.

Features	**Students (n = 1656)**		**Faculty Members (n = 159)**		**Total (n = 1815)**	
	Yes	***NO***	***Yes***	***NO***	***Yes***	***NO***
1	*2*	*3*	*4*	*5*	*6*	*7*
Navigation is easy through the links or menus	1428 (86.2)	228 (13.8)	152 (95.6)	7 (4.4)	1580 (87.1)	235 (12.9)

Includes a site map	171 (10.3)	1485 (89.7)	18 (11.3)	141 (88.7)	189 (10.4)	1626 (89.6)
Includes internal search engine	401 (24.2)	1255 (75.8)	43 (27.0)	116 (73.0)	444 (24.5)	1371 (75.5)
Links are meaningful and relevant to the subject	1380 (83.3)	276 (16.7)	152 (95.6)	7 (4.4)	1532 (84.4)	283 (15.6)

Note: Col.2–Col.7: Figures in Parentheses indicate percentage.

Table 5. User support features.

Features	**Students (n=1656)**		**Faculty Members (n = 159)**		**Total (n = 1815)**		**$\chi 2$ value df = 1 TV = 3.84**
	Yes	***NO***	***Yes***	***NO***	***Yes***	***NO***	
1	*2*	*3*	*4*	*5*	*6*	*7*	*8*
Feedback/suggestion forum is available	448 (27.1)	1208 (72.9)	41 (25.8)	118 (74.2)	489 (26.9)	1326 (73.1)	0.118@ (0.731)
Frequently Asked Question (FAQs)	90 (5.4)	1566 (94.6)	8 (5.0)	151 (95.0)	98 (5.4)	1717 (94.6)	0.046@ (0.830)
Link to social network sites	945 (57.1)	711 (42.9)	87 (54.7)	72 (45.3)	1032 (56.9)	783 (43.1)	0.326@ (0.568)
Login facility	928 (56.0)	728 (44.0)	84 (52.8)	75 (47.2)	1012 (55.8)	803 (44.2)	0.605@ (0.437)

Note: 1. Col.2–Col.7: Figures in parentheses indicate percentage; Col 8: Figures in parentheses indicates probability values;
2. @ Not significant.

Table 4 shows that majority of the respondents replied that navigation features namely navigation is easy through the links or menus (87.1 percent) and links are meaningful and relevant to the subject (84.4 percent) at their respective websites. Nearly one-fourth of them (24.5 percent) replied that websites provided internal search facility and over a one-tenth of them (10.4 percent) replied that site map has provided by of the college websites.

User Support Features

User support is another criteria used to evaluate the home pages of the college websites. The respondent's statement of provision of user support facilities in home pages of college websites has been shown in Table 5.

Table 5 shows that more than half of the respondents replied that user support features namely link to social network sites (56.9 percent) and login facility (55.8 percent) provided by their respective websites. More than one-fourth of them (26.9 percent) responded feedback/suggestion forum provided by their respective websites. A meagre percent of them replied that FAQs provided by their college websites. A Similar study done by Shivabasappa [21] shows that nearly half of the users have rated FAQs feature as good and very good whereas, slightly more than two-fifths of the users have rated feedback as good and very good.

Overall Features of Websites

Some of the essential features of the websites are analyzed using nine important variables. The respondents were asked to mark their opinion on a five point scale. The percentage is calculated based on the preference given by the respondents. ANOVA test was used to compare the observed results in Table 6.

Table 6. Overall features.

Features	**Students (n = 1656)**					**Faculty Members (n = 159)**					**Total (n = 1815)**				
	Ex	*V G*	*G*	*F*	*P*	*Ex*	*V G*	*G*	*F*	*P*	*Ex*	*V G*	*G*	*F*	*P*
Accessibility	95 (5.7)	283 (17.1)	861 (52.0)	287 (96.3)	130 (7.9)	22 (13.8)	49 (30.8)	77 (48.4)	11 (6.9)	-	117 (6.4)	332 (18.3)	938 (51.7)	298 (16.4)	130 (7.2)
Accuracy	130 (7.9)	372 (22.5)	751 (45.4)	292 (17.6)	111 (6.7)	18 (11.3)	58 (36.5)	69 (43.4)	13 (8.2)	1 (0.6)	148 (8.2)	430 (23.7)	820 (45.2)	305 (16.8)	112 (6.2)
Authority	163	354	755	288	96	33	50	60	16	-	196	404	815	304	96

	(9.8)	(21.4)	(45.6)	(17.4)	(5.8)	(20.8)	(31.4)	(37.7)	(10.1)		(10.8)	(22.3)	(44.9)	(16.7)	(5.3)
Consistency	128 (7.7)	372 (22.5)	784 (47.3)	278 (16.8)	94 (5.7)	18 (11.3)	47 (29.6)	72 (45.3)	20 (12.6)	2 (1.3)	146 (8.0)	419 (23.1)	856 (47.2)	298 (16.4)	96 (5.3)
Permanence	121 (7.3)	364 (22.0)	784 (47.3)	299 (18.1)	88 (5.3)	16 (10.1)	52 (32.7)	65 (40.9)	26 (16.4)	-	137 (7.5)	416 (22.9)	849 (46.8)	325 (17.9)	88 (4.8)
Ease to Use	169 (10.2)	494 (29.8)	642 (38.8)	251 (15.2)	100 (6.0)	22 (13.8)	68 (42.8)	60 (37.7)	9 (5.7)	-	191 (10.5)	562 (31.0)	702 (38.7)	260 (14.3)	100 (5.5)
Timeliness	121 (7.3)	316 (19.1)	762 (46.0)	324 (19.6)	133 (8.0)	23 (14.5)	44 (27.7)	63 (39.6)	28 (17.6)	1 (0.6)	144 (7.9)	360 (19.8)	825 (45.5)	352 (19.4)	134 (7.4)
Uniqueness	151 (9.1)	382 (23.1)	695 (42.0)	273 (16.5)	155 (9.4)	25 (15.7)	50 (31.4)	54 (34.0)	27 (17.0)	3 (1.9)	176 (9.7)	432 (23.8)	749 (41.3)	300 (16.5)	158 (8.7)
Usefulness	232 (14.0)	437 (26.4)	642 (38.8)	254 (15.3)	91 (5.5)	30 (18.9)	52 (32.7)	60 (37.7)	15 (9.4)	2 (1.3)	262 (14.4)	489 (26.9)	702 (38.7)	269 (14.8)	93 (5.1)

Note : Ex: Excellent; VG: Very Good; G: Good; F: Fair; P: Poor;
(Figures in parentheses indicate percentage)

ANOVA

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between groups	4343478.28	9	482608.70	412.17	0.00**	1.999115
Within groups	93672.22	80	1170.90			
Total	4437150.50	89				

***significant at 1 percent level.*

Table 6 reveals that accessibility is rated as good by more than half of the users (51.7 percent) followed by Consistency (47.2 percent) and Permanence (46.8 percent) features. A similar study was carried out by Kothainayaki [6] revealed that authority is the feature which is most expected from the academic websites. It is followed by accuracy and accessibility features. The least expected is the consistency features in academic websites URLs.

The study reveals that nearly four-fifths of the respondents (79.9 percent) rated accuracy of the website between good and very good. A similar study was done by Shivabasappa [21], shows accuracy on the library websites have been rated as good and very good by nearly three-fourths of the users. The study reveals that nearly two-third of the users (61.6 percent) rated authority as good and very good. Result of the present study supported the study conducted by Kothainayaki [6], in which most of the LIS professionals working in all types of institutions consider the authority feature as essential.

Nearly two-fifth of respondents (38.7 percent) rated ‘ease to use’ as good. It also reveals that a good number of the users (45.5 percent) rated timeliness of website as good. Over two-fifths of the respondents (41.3 percent) opined that uniqueness of their respective websites as good. More than two-fifth of the students rated it as good whereas over a one-third of the faculty members rated it as good. Nearly two-fifth of the respondents (38.7 percent) opined that usefulness of the website as good and over one-fourth of them (26.9 percent) rated it as very good. There is a statistically significant difference between students and faculty members in their opinions with regard to overall features of website. It is determined by one-way ANOVA.

Suggestions to Enhance the Quality of the Website

Based on the findings of the study the following suggestions are put forward to enhance the quality of the website:

- A few colleges provided information about date of last updated. Therefore, it should be mandatory to update websites regularly.
- The college website should cover maximum content covering hyperlinks systematically placed on the page. At the same time, the page should not be overcrowded with the hyperlinks. To avoid overcrowding look, pop up links can be used.
- It should be easy to navigate. Each internal link should cover the link for college home page.

- Search facility provided by 13.72 percent of the colleges and sitemap provided by 13 percent of them. A very few colleges (0.72 percent) are provided FAQ's. Hence, FAQs, sitemap and search facility should be added to the website, which will increase its accessibility.
- Over one-fourth (27.24 percent) of college web sites have separate 'Library link' on the home page. Therefore, engineering college website should include a separate 'library' link.
- None of the college have separate library home page. Hence, the colleges should include a separate library home page.
- Some standards for designing engineering college websites should be evolved.

CONCLUSION

College websites contain educational features which aim to provide the information and services to its stakeholders in different ways. To achieve these goals, the college website design must go through a number of guidelines for the design to ensure that users are more satisfied with the services of these sites services. The homepages of the college website should be constructed logically, and periodically evaluated using criteria such as access, contact information, authority, currency, content, ease of navigation, etc. College webmaster should pay more attention to the college web design and content making them more attractive to the user community. It would be useful to carry out a more comprehensive study covering more institutions and more diagnosis tools to measure the evaluation criteria of the college websites in Andhra Pradesh.

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APPENDIX

Top 20 Colleges based on Evaluation Criteria

Code	Rank	Name of the College/University
GU	1	GITAM University
KLU	2	K.L. University
GEC	3	Gudlavalleru Engineering College
ACE	4	Audishankara College of Engineering and Technology
VRSEC	5	Velagapudi Ramakrishna Siddhartha Engineering College
RVR	6	RVR & JC College of Engineering
SVE	7	Sri Vasavi Engineering College
ANIT	8	Anil Neerukonda Institute of Technology & Science
PBRV	9	Parvatha Reddy Babul Reddy Visvodaya Institute of Technology and Science
SITE	10	Sasi Institute of Technology & Engineering
MITS	11	Madanapalle Institute of Technology and Science
SVUE	12	Sri Venkateswara University College of Engineering
GPEC	13	G. Pulla Reddy Engineering College
RMCE	14	Rajeev Gandhi Memorial College of Engineering and Technology
AIT	15	Audisankara Institute of Technology
VU	16	Vignan University
ANUE	17	Aharya Nagarjuna University College of Engineering
DCT	18	Devineni Venkata Ramana & Dr. Himasekhar MIC College of Technology
SVEW	19	Shri Vishnu Engineering College for Women
AUEW	20	Andhra University College of Engineering for Women

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Coupled fixed points of generalized rational type $\mathcal{Z}$-contraction maps in b-metric spaces

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Abstract

In this paper, we introduce generalized rational type $\mathcal{Z}$-contraction maps for a single map $f : X \times X \to X$ where X is a b-metric space and prove the existence and uniqueness of coupled fixed points. We extend it to a pair of maps by defining generalized rational type $\mathcal{Z}$-contraction pair of maps and prove the existence of common coupled fixed points in complete b-metric spaces. We provide examples in support of our results.

Keywords: coupled fixed points, b-metric space, generalized rational type $\mathcal{Z}$-contraction maps.
2020 MSC: 47H10, 54H25.

1 Introduction

Banach contraction principle plays an important role in solving nonlinear functional analysis. In the direction of generalization of contraction condition, Dass and Gupta [13] initiated a contraction condition involving rational expression and established the existence of fixed points in complete metric spaces.

In the direction of generalization of metric spaces, Bourbaki [10] and Bakhtin [5] initiated the idea of b-metric spaces. The concept of b-metric space or metric type space was introduced by Czerwik [11] as a generalization of metric space. Afterwards, many authors studied the existence of fixed points for a single-valued and multi-valued mappings in b-metric spaces under certain contraction conditions. For more details, we refer [2, 3, 8, 9, 12, 14, 16, 18, 23, 24].

In 2006, Bhaskar and Lakshmikantham [6] introduced the notion of coupled fixed point and established the existence of coupled fixed points for mixed monotone mappings in ordered metric spaces. Later, Lakshmikantham and Ćirić [19] introduced the notion of coupled coincidence points of mappings in two variables. Afterwards, many authors studied coupled fixed point theorems, we refer [20, 22, 25, 26].

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2 Preliminaries

Definition 2.1. [11] Let X be a non-empty set. A function $d : X \times X \to [0, \infty)$ is said to be a b-metric if the following conditions are satisfied: for any $x, y, z \in X$

(i) $0 \leq d(x, y)$ and $d(x, y) = 0$ if and only if $x = y$,
(ii) $d(x, y) = d(y, x)$,
(iii) there exists $s \geq 1$ such that $d(x, z) \leq s[d(x, y) + d(y, z)]$.

In this case, the pair (X, d) is called a b-metric space with coefficient s.

Every metric space is a b-metric space with $s = 1$. In general, every b-metric space is not a metric space.

Definition 2.2. [9] Let (X, d) be a b-metric space.

(i) A sequence $\{x_n\}$ in X is called b-convergent if there exists $x \in X$ such that $d(x_n, x) \to 0$ as $n \to \infty$. In this case, we write $\lim_{n\to\infty} x_n = x$.
(ii) A sequence $\{x_n\}$ in X is called b-Cauchy if $d(x_n, x_m) \to 0$ as $n, m \to \infty$.
(iii) A b-metric space (X, d) is said to be a complete b-metric space if every b-Cauchy sequence in X is b-convergent in X.
(iv) A set $B \subset X$ is said to be b-closed if for any sequence $\{x_n\}$ in B such that $\{x_n\}$ is b-convergent to $z \in X$ then $z \in B$.

In general, a b-metric is not necessarily continuous.

In this paper, we denote $\mathbb{R}^+ = [0, \infty)$ and $\mathbb{N}$ is the set of all natural numbers.

Example 2.3. [15] Let $X = \mathbb{N} \cup \{\infty\}$. We define a mapping $d : X \times X \to \mathbb{R}^+$ as follows:

$$d(m, n) = \begin{cases} 0 & \text{if } m = n, \\ |\frac{1}{m} - \frac{1}{n}| & \text{if one of } m, n \text{ is even and the other is even or } \infty, \\ 5 & \text{if one of } m, n \text{ is odd and the other is odd or } \infty, \\ 2 & \text{otherwise.} \end{cases}$$

Then (X, d) is a b-metric space with coefficient $s = \frac{5}{2}$.

Definition 2.4. [9] Let (X, d_X) and (Y, d_Y) be two b-metric spaces. A function $f : X \to Y$ is a b-continuous at a point $x \in X$, if it is b-sequentially continuous at x. i.e., whenever $\{x_n\}$ is b-convergent to x we have fx_n is b-convergent to fx.

Definition 2.5. [6] Let X be a nonempty set and $f : X \times X \to X$ be a mapping. Then we say that an element $(x, y) \in X \times X$ is a coupled fixed point, if $f(x, y) = x$ and $f(y, x) = y$.

Definition 2.6. [19] Let X be a nonempty set. Let $F : X \times X \to X$ and $g : X \to X$ be two mappings. An element $(x, y) \in X \times X$ ia called

(i) a coupled coincidence point of the mappings F and g if $F(x, y) = gx$ and $F(y, x) = gy$;
(ii) a common coupled fixed point of mappings F and g if $F(x, y) = gx = x$ and $F(y, x) = gy = y$.

The following lemma is useful in proving our main results.

Lemma 2.7. [1] Let (X, d) be a b-metric space with coefficient $s \geq 1$. Suppose that $\{x_n\}$ and $\{y_n\}$ are b-convergent to x and y respectively. Then we have

$$\frac{1}{s^2} d(x, y) \leq \liminf_{n\to\infty} d(x_n, y_n) \leq \limsup_{n\to\infty} d(x_n, y_n) \leq s^2 d(x, y).$$

In particular, if $x = y$, then we have $\lim_{n\to\infty} d(x_n, y_n) = 0$. Moreover for each $z \in X$ we have

$$\frac{1}{s} d(x, z) \leq \liminf_{n\to\infty} d(x_n, z) \leq \limsup_{n\to\infty} d(x_n, z) \leq s d(x, z).$$

In 2015, Khojasteh, Shukla and Radenović [17] introduced simulation function and defined $\mathcal{Z}$-contraction with respect to a simulation function.

Definition 2.8. [17] A simulation function is a mapping $\zeta : \mathbb{R}^+ \times \mathbb{R}^+ \to (-\infty, \infty)$ satisfying the following conditions:
(ζ_1) $\zeta(0,0) = 0$;
(ζ_2) $\zeta(t,s) < s - t$ for all $s, t > 0$;
(ζ_3) if $\{t_n\}, \{s_n\}$ are sequences in $(0,\infty)$ such that $\lim_{n\to\infty} t_n = \lim_{n\to\infty} s_n = l \in (0,\infty)$ then $\limsup_{n\to\infty} \zeta(t_n, s_n) < 0$.

Remark 2.9. [4] Let ζ be a simulation function. If $\{t_n\}, \{s_n\}$ are sequences in $(0,\infty)$ such that $\lim_{n\to\infty} t_n = \lim_{n\to\infty} s_n = l \in (0,\infty)$ then $\limsup_{n\to\infty} \zeta(kt_n, s_n) < 0$ for any $k > 1$.

The following are examples of simulation functions.

Example 2.10. [4] Let $\zeta : \mathbb{R}^+ \times \mathbb{R}^+ \to (-\infty, \infty)$ be defined by
(i) $\zeta(t,s) = \lambda s - t$ for all $t, s \in \mathbb{R}^+$, where $\lambda \in [0,1)$;
(ii) $\zeta(t,s) = \frac{s}{1+s} - t$ for all $s, t \in \mathbb{R}^+$;
(iii) $\zeta(t,s) = s - kt$ for all $t, s \in \mathbb{R}^+$, where $k > 1$;
(iv) $\zeta(t,s) = \frac{1}{1+s} - (1+t)$ for all $s, t \in \mathbb{R}^+$;
(v) $\zeta(t,s) = \frac{1}{k+s} - t$ for all $s, t \in \mathbb{R}^+$ where $k > 1$.

Definition 2.11. [17] Let (X,d) be a metric space and $f : X \to X$ be a selfmap of X. We say that f is a $\mathcal{Z}$-contraction with respect to ζ if there exists a simulation function ζ such that

$$\zeta(d(fx, fy), d(x,y)) \geq 0 \quad \text{for all} \quad x, y \in X.$$

Theorem 2.12. [17] Let (X,d) be a complete metric space and $f : X \to X$ be a $\mathcal{Z}$-contraction with respect to a certain simulation function ζ. Then for every $x_0 \in X$, the Picard sequence $\{f^n x_0\}$ converges in X and $\lim_{n\to\infty} f^n x_0 = u$(say) in X and u is the unique fixed point of f in X.

Recently, Olgun, Bicer and Alyildiz [21] proved the following result in complete metric spaces.

Theorem 2.13. [21] Let (X,d) be a complete metric space and $f : X \to X$ be a selfmap on X. If there exists a simulation function ζ such that

$$\zeta(d(fx, fy), M(x,y)) \geq 0$$

for all $x, y \in X$, where $M(x,y) = \max\{d(x,y), d(x,fx), d(y,fy), \frac{d(x,fy)+d(y,fx)}{2}\}$,then for every $x_0 \in X$, the Picard sequence $\{f^n x_0\}$ converges in X and $\lim_{n\to\infty} f^n x_0 = u$(say) in X and u is the unique fixed point of f in X.

In 2018, Babu, Dula and Kumar [4] extended Theorem 1.13 [21] to pair of selfmaps in the setting of b-metric spaces as follows.

Theorem 2.14. [4] Let (X,d) be a complete b-metric space with coefficient $s \geq 1$ and $f, g : X \to X$ be a selfmaps on X. If there exists a simulation function ζ such that

$$\zeta(s^4 d(fx, gy), M(x,y)) \geq 0$$

for all $x, y \in X$, where $M(x,y) = \max\{d(x,y), d(x,fx), d(y,gy), \frac{d(x,gy)+d(y,fx)}{2s}\}$, then f and g have a unique common fixed point in X, provided either f or g is b-continuous.

Recently, Bindu and Malhotra [7] proved the existence of common coupled fixed points as follows:

Theorem 2.15. Let (X,d) be a complete b-metric space with parameter $s \geq 1$ and let the mappings $S, T : X \times X \to X$ satisfy

$$\begin{aligned} d(S(x,y), T(u,v)) \leq{}& \alpha_1 \tfrac{d(x,u)+d(y,v)}{2} + \alpha_2 \tfrac{d(x,S(x,y))d(u,T(u,v))}{1+d(x,u)+d(y,v)+d(u,S(x,y))} + \alpha_3 \tfrac{d(u,S(x,y))d(x,T(u,v))}{1+d(x,u)+d(y,v)+d(u,S(x,y))} \\ &+ \alpha_4 \tfrac{d(S(x,y),T(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,S(x,y))} + \alpha_5 \tfrac{d(S(x,y),T(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,S(x,y))} \\ &+ \alpha_6 \tfrac{d(u,T(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,S(x,y))} + \alpha_7 \tfrac{d(u,S(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,S(x,y))} \\ &+ \alpha_8 \tfrac{d(u,S(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,S(x,y))} + \alpha_9 \max d(u,S(x,y)), d(S(x,y),T(u,v)) \end{aligned}$$

for all $x, y, u, v \in X$ and $\alpha_i \geq 0, i = 1, 2, \ldots, 9$ with $s\alpha_1 + \alpha_2 + \alpha_4 + \alpha_5 + \alpha_6 + s\alpha_9 < 1$ and $\alpha_1 + \alpha_3 + \alpha_4 + \alpha_5 + \alpha_7 + \alpha_8 + \alpha_9 < 1$. Then S and T have a unique common coupled fixed point in X.

Motivated by the works of Bindu and Malhotra [7], in Section 3, we introduce generalized rational type $\mathcal{Z}$-contraction maps for a single map $f : X \times X \to X$ where X is a b-metric space and we extend it to a pair of maps. In Section 4, we prove the existence and uniqueness of coupled fixed points and common coupled fixed points in complete b-metric spaces. Examples are provided in support of our results in Section 5.

3 Generalized rational type $\mathcal{Z}$-contraction maps

The following we introduce generalized rational type $\mathcal{Z}$-contraction maps for a single and a pair of maps in b-metric spaces as follows:

Definition 3.1. Let (X, d) be a b-metric space with coefficient $s \geq 1$ and $f : X \times X \to X$ be a map. We say that f is a generalized rational type $\mathcal{Z}$-contraction map, if there exists a simulation function ζ such that

$$\zeta(s^3 d(f(x,y), f(u,v)), M(x,y,u,v)) \geq 0 \quad \text{for all } x,y,u,v \in X, \tag{3.1}$$

where

$$\begin{aligned} M(x,y,u,v) = \max\{&\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\max\{d(u,f(x,y)), d(f(x,y),f(u,v))\}\}. \end{aligned}$$

Remark 3.2. It is clear that from definition of simulation function that $\zeta(a,b) < 0$, for all $a \geq b > 0$. Therefore if f satisfies (3.1), then

$$s^3 d(f(x,y), f(u,v)) < M(x,y,u,v), \text{ for all } x,y,u,v \in X.$$

Example 3.3. Let $X = [0,1]$ and let $d : X \times X \to \mathbb{R}^+$ defined by

$$d(x,y) = \begin{cases} 0 & \text{if } x = y \\ (x+y)^2 & \text{if } x \neq y. \end{cases}$$

Then clearly (X, d) is a b-metric space with coefficient $s = 2$. We define $f : X \times X \to X$ by $f(x,y) = \frac{\log(1+x^2+y^2)}{16}$ for all $x \in [0,1]$ and

$$\zeta : \mathbb{R}^+ \times \mathbb{R}^+ \to (-\infty, \infty) \quad \text{by} \quad \zeta(t,s) = \frac{1}{2}s - t, t \geq 0, s \geq 0.$$

We have $s^3 d(f(x,y), f(u,v)) = 8[\frac{\log(1+x^2+y^2)}{16} + \frac{\log(1+u^2+v^2)}{16}]^2$

$$\begin{aligned} &\leq \tfrac{1}{8}[(x+u)^2 + (y+v)^2] \\ &= \tfrac{1}{2}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{1}{2}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\qquad \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\qquad \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\qquad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\qquad \max\{d(u,f(x,y)), d(f(x,y),f(u,v))\}\}). \end{aligned}$$

Therefore f is a generalized rational type $\mathcal{Z}$-contraction map.

Definition 3.4. Let (X, d) be a b-metric space with coefficient $s \geq 1$ and $f, g : X \times X \to X$ be two maps. We say that the pair (f, g) is a generalized rational type $\mathcal{Z}$-contraction maps, if there exists a simulation function ζ such that

$$\zeta(s^3 d(f(x,y), g(u,v)), M(x,y,u,v)) \geq 0, \text{ for all } x,y,u,v \in X, \tag{3.2}$$

where

$$\begin{aligned} M(x,y,u,v) = \max\{&\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\max\{d(u,f(x,y)), d(f(x,y),g(u,v))\}\}. \end{aligned}$$

Remark 3.5. It is clear that from definition of simulation function that $\zeta(a,b)<0$, for all $a\geq b>0$. Therefore if f satisfies (3.2), then

$$s^3d(f(x,y),g(u,v))<M(x,y,u,v),\ \text{ for }\ \text{all } x,y,u,v\in X.$$

Example 3.6. Let $X=[0,1]$ and let $d:X\times X\to\mathbb{R}^+$ defined by

$$d(x,y)=\begin{cases}0 & \text{if } x=y\\ (x+y)^2 & \text{if } x\neq y.\end{cases}$$

Then clearly (X,d) is a b-metric space with coefficient $s=2$. We define $f,g:X\times X\to X$ by

$$f(x,y)=\begin{cases}\frac{\log(1+x+y)}{16} & \text{if } x,y\in[0,\frac{1}{2})\\ \frac{1}{32} & \text{if } x,y\in[\frac{1}{2},1]\end{cases}\quad\text{and}\quad g(x,y)=\begin{cases}\frac{xe^y}{8} & \text{if } x,y\in[0,\frac{1}{2})\\ \log(x+y) & \text{if } x,y\in[\frac{1}{2},1].\end{cases}$$

$\zeta:\mathbb{R}^+\times\mathbb{R}^+\to(-\infty,\infty)$ by $\zeta(t,s)=\frac{99}{100}s-t, t\geq 0, s\geq 0$.

Case (i). $x,y,u,v\in[0,\frac{1}{2})$.

$$\begin{aligned}s^3d(f(x,y),g(u,v)) &= 8[\tfrac{\log(1+x+y)}{16}+\tfrac{ue^v}{8}]^2\\ &\leq \tfrac{99}{400}[(x+u)^2+(y+v)^2]\\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s})\\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s},\tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \max\{d(u,f(x,y)),d(f(x,y),g(u,v))\}\}).\end{aligned}$$

Case (ii). $x,y,u,v\in[\frac{1}{2},1]$.

$$\begin{aligned}s^3d(f(x,y),g(u,v)) &= 8[\tfrac{1}{32}+\log(u+v)]^2\\ &\leq \tfrac{99}{400}[(x+u)^2+(y+v)^2]\\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s})\\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s},\tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \max\{d(u,f(x,y)),d(f(x,y),g(u,v))\}\})\end{aligned}$$

Case (iii). $x,y\in[\frac{1}{2},1], u,v\in[0,\frac{1}{2})$.

$$\begin{aligned}s^3d(f(x,y),g(u,v)) &= 8[\tfrac{1}{16}+\tfrac{ue^v}{4}]^2\\ &\leq \tfrac{99}{400}[(x+u)^2+(y+v)^2]\\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s})\\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s},\tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \max\{d(u,f(x,y)),d(f(x,y),g(u,v))\}\})\end{aligned}$$

Case (iv). $x,y\in[0,\frac{1}{2}), u,v\in[\frac{1}{2},1]$.

$$\begin{aligned}s^3d(f(x,y),g(u,v)) &= 8[\tfrac{\log(1+x+y)}{8}+\log(x+y)]^2\\ &\leq \tfrac{99}{400}[(x+u)^2+(y+v)^2]\\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s})\\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s},\tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},\\ &\quad \max\{d(u,f(x,y)),d(f(x,y),g(u,v))\}\}).\end{aligned}$$

Therefore the pair (f,g) is a generalized rational type $\mathcal{Z}$-contraction maps.

4 Main results

Theorem 4.1. Let (X,d) be a complete b-metric space with coefficient $s\geq 1$ and $f:X\times X\to X$ be a rational type $\mathcal{Z}$-contraction map. Then f has a unique coupled fixed point in X.

Proof . Let x_0 and y_0 be arbitrary points in X. We define $x_{i+1} = f(x_i, y_i)$ and $y_{i+1} = f(y_i, x_i)$ for $i = 0, 1, 2, \ldots$. We consider

$$\zeta(s^3 d(x_{n+1}, x_{n+2}), M(x_n, y_n, x_{n+1}, y_{n+1})) = \zeta(s^3 d(f(x_n, y_n), f(x_{n+1}, y_{n+1})), M(x_n, y_n, x_{n+1}, y_{n+1})) \geq 0, \tag{4.1}$$

where

$$\begin{aligned}
M(x_n, y_n, x_{n+1}, y_{n+1}) &= \max\{\tfrac{d(x_n,x_{n+1})+d(y_n,y_{n+1})}{2s}, \tfrac{d(x_n,f(x_n,y_n))d(x_{n+1},f(x_{n+1},y_{n+1}))}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))},\\
&\tfrac{d(x_{n+1},f(x_n,y_n))d(x_n,f(x_{n+1},y_{n+1}))}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))}, \tfrac{d(f(x_n,y_n),f(x_{n+1},y_{n+1}))d(x_n,x_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))},\\
&\tfrac{d(f(x_n,y_n),f(x_{n+1},y_{n+1}))d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))}, \tfrac{d(x_{n+1},f(x_{n+1},y_{n+1}))d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))},\\
&\tfrac{d(x_{n+1},f(x_n,y_n))d(x_n,x_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))}, \tfrac{d(x_{n+1},f(x_n,y_n))d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},f(x_n,y_n))},\\
&\max\{d(x_{n+1}, f(x_n, y_n)), d(f(x_n, y_n), f(x_{n+1}, y_{n+1}))\}\}\\
&= \max\{\tfrac{d(x_n,x_{n+1})+d(y_n,y_{n+1})}{2s}, \tfrac{d(x_n,x_{n+1})d(x_{n+1},x_{n+2})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})},\\
&\tfrac{d(x_{n+1},x_{n+1})d(x_n,x_{n+2})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})}, \tfrac{d(x_{n+1},x_{n+2})d(x_n,x_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})},\\
&\tfrac{d(x_{n+1},x_{n+2})d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})}, \tfrac{d(x_{n+1},x_{n+2})d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})},\\
&\tfrac{d(x_{n+1},x_{n+1})d(x_n,x_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})}, \tfrac{d(x_{n+1},x_{n+1})d(y_n,y_{n+1})}{1+d(x_n,x_{n+1})+d(y_n,y_{n+1})+d(x_{n+1},x_{n+1})},\\
&\max\{d(x_{n+1}, x_{n+1}), d(x_{n+1}, x_{n+2})\}\}\\
&\leq \max\{\tfrac{d(x_n,x_{n+1})+d(y_n,y_{n+1})}{2s}, d(x_{n+1}, x_{n+2})\}.
\end{aligned}$$

If $M(x_n, y_n, x_{n+1}, y_{n+1}) = d(x_{n+1}, x_{n+2})$ then from (4.1), we have

$$\begin{aligned}
0 \leq \zeta(s^3 d(x_{n+1}, x_{n+2}), M(x_n, y_n, x_{n+1}, y_{n+1})) &= \zeta(s^3 d(x_{n+1}, x_{n+2}), d(x_{n+1}, x_{n+2}))\\
&< d(x_{n+1}, x_{n+2}) - s^3 d(x_{n+1}, x_{n+2}),
\end{aligned}$$

which is a contradiction. Therefore

$$d(x_{n+1}, x_{n+2}) \leq \frac{d(x_n, x_{n+1}) + d(y_n, y_{n+1})}{2s} \tag{4.2}$$

for all $n = 0, 1, 2, \ldots$. Similarly, we can prove that

$$d(y_{n+1}, y_{n+2}) \leq \frac{d(y_n, y_{n+1}) + d(x_n, x_{n+1})}{2s} \tag{4.3}$$

for all $n = 0, 1, 2, \ldots$. Adding the inequalities (4.2) and (4.3), we have

$$d(x_{n+1}, x_{n+2}) + d(y_{n+1}, y_{n+2}) \leq h[d(x_n, x_{n+1}) + d(y_n, y_{n+1})],$$

where $h = \frac{1}{2s} < 1$. Also, it is easy to see that

$$d(x_n, x_{n+1}) + d(y_n, y_{n+1}) \leq h[d(x_{n-1}, x_n) + d(y_{n-1}, y_n)].$$

Therefore

$$d(x_{n+1}, x_{n+2}) + d(y_{n+1}, y_{n+2}) \leq h^2[d(x_{n-1}, x_n) + d(y_{n-1}, y_n)].$$

Continuing in the same way, we get that

$$d(x_{n+1}, x_{n+2}) + d(y_{n+1}, y_{n+2}) \leq h^n[d(x_0, x_1) + d(y_0, y_1)].$$

For $m > n, m, n \in \mathbb{N}$, we have

$$\begin{aligned}
d(x_n, x_m) + d(y_n, y_m) &\leq s[d(x_n, x_{n+1}) + d(x_{n+1}, x_m)] + s[d(y_n, y_{n+1}) + d(y_{n+1}, y_m)]\\
&\leq s[d(x_n, x_{n+1}) + d(y_n, y_{n+1})] + s^2[d(x_{n+1}, x_{n+2}) + d(x_{n+2}, x_m)]\\
&\quad + s^2[d(y_{n+1}, y_{n+2}) + d(y_{n+2}, y_m)]\\
&= s[d(x_n, x_{n+1}) + d(y_n, y_{n+1})] + s^2[d(x_{n+1}, x_{n+2}) + d(y_{n+1}, y_{n+2})]\\
&\quad + s^2[d(x_{n+2}, x_m) + d(y_{n+2}, y_m)] \ldots + s^{m-n}[d(x_{m-1}, x_m) + d(y_{m-1}, y_m)]\\
&\leq [sh^n + s^2h^{n+1} + \ldots + s^{m-n}h^{m-1}][d(x_0, x_1) + d(y_0, y_1)]\\
&\leq sh^n[1 + sh + (sh)^2 \ldots + (sh)^{m-1} + \ldots][d(x_0, x_1) + d(y_0, y_1)]\\
&= sh^n(\tfrac{1}{1-sh})[d(x_0, x_1) + d(y_0, y_1)] \to 0 \text{ as } n \to \infty.
\end{aligned}$$

Therefore $\{x_n\}$ and $\{y_n\}$ are b-Cauchy sequences in X. Since X is b-complete, there exist $x, y \in X$ such that $x_n \to x$ and $y_n \to y$ as $n \to \infty$. We now prove that $x = f(x, y)$ and $y = f(y, x)$. On the contrary suppose that $x \neq f(x, y)$ and $y \neq f(y, x)$. We now consider

$$\zeta(s^3 d(f(x, y), x_{n+1}), M(x, y, x_n, y_n)) = \zeta(s^3 d(f(x, y), f(x_n, y_n)), M(x, y, x_n, y_n)) \geq 0, \tag{4.4}$$

where $M(x,y,x_n,y_n) = \max\{\frac{d(x,x_n)+d(y,y_n)}{2s}, \frac{d(x,f(x,y))d(x_n,f(x_n,y_n))}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(x_n,f(x,y))d(x,f(x_n,y_n))}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(f(x,y),f(x_n,y_n))d(x,x_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(f(x,y),f(x_n,y_n))d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(x_n,f(x_n,y_n))d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(x_n,f(x,y))d(x,x_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(x_n,f(x,y))d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\max\{d(x_n,f(x,y)), d(f(x,y),f(x_n,y_n))\}\}$
$= \max\{\frac{d(x,x_n)+d(y,y_n)}{2s}, \frac{d(x,f(x,y))d(x_n,x_{n+1})}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(x_n,f(x,y))d(x,x_{n+1})}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(f(x,y),x_{n+1})d(x,x_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(f(x,y),x_{n+1})d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(x_n,x_{n+1})d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\frac{d(x_n,f(x,y))d(x,x_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))}, \frac{d(x_n,f(x,y))d(y,y_n)}{1+d(x,x_n)+d(y,y_n)+d(x_n,f(x,y))},$
$\max\{d(x_n,f(x,y)), d(f(x,y),x_{n+1})\}\}.$

On taking limit superior as $n \to \infty$ in $M(x,y,x_n,y_n)$, we have

$$\limsup_{n\to\infty} M(x,y,x_n,y_n) \leq sd(x,f(x,y)).$$

On letting limit superior as $n \to \infty$ in (4.4) and using the Lemma 2.7, we have

$0 \leq \limsup_{n\to\infty} \zeta(s^3 d(f(x,y),x_{n+1}), M(x,y,x_n,y_n))$
$= \limsup_{n\to\infty} M(x,y,x_n,y_n) - \liminf_{n\to\infty} s^3 d(f(x,y),x_{n+1})$
$\leq d(x,f(x,y)) - s^3 \frac{d(x,f(x,y))}{s},$

a contradiction. Therefore $x = f(x,y)$. Similarly we can prove that $y = f(y,x)$. Therefore (x,y) is a coupled fixed point of f. Let $(x',y') \in X \times X$ be another coupled fixed point of f with $(x',y') \neq (x,y)$. We consider

$$\zeta(s^3 d(x,x'), M(x,y,x',y')) = \zeta(s^3 d(f(x,y),f(x',y')), M(x,y,x',y')) \geq 0,$$

where

$M(x,y,x',y') = \max\{\frac{d(x,x')+d(y,y')}{2s}, \frac{d(x,f(x,y))d(x',f(x',y'))}{1+d(x,x')+d(y,y')+d(x',f(x,y))}, \frac{d(x',f(x,y))d(x,f(x',y'))}{1+d(x,x')+d(y,y')+d(x',f(x,y))},$
$\frac{d(f(x,y),f(x',y'))d(x,x')}{1+d(x,x')+d(y,y')+d(x',f(x,y))}, \frac{d(f(x,y),f(x',y'))d(y,y')}{1+d(x,x')+d(y,y')+d(x',f(x,y))},$
$\frac{d(x',f(x',y'))d(y,y')}{1+d(x,x')+d(y,y')+d(x',f(x,y))}, \frac{d(x',f(x,y))d(x,x')}{1+d(x,x')+d(y,y')+d(x',f(x,y))},$
$\frac{d(x',f(x,y))d(y,y')}{1+d(x,x')+d(y,y')+d(x',f(x,y))}, \max\{d(x',f(x,y)), d(f(x,y),f(x',y'))\}\}$
$\leq \max\{\frac{d(x,x')+d(y,y')}{2s}, d(x,x')\}.$

If $M(x,y,x',y') = d(x,x')$ then we have

$$\zeta(s^3 d(x,x'), M(x,y,x',y')) = d(x,x') - s^3 d(x,x') \geq 0,$$

which is a contradiction. Therefore

$$d(x,x') \leq \frac{d(x,x')+d(y,y')}{2s}. \tag{4.5}$$

Similarly, we can prove that

$$d(y,y') \leq \frac{d(x,x')+d(y,y')}{2s}.. \tag{4.6}$$

Adding the inequalities (4.5) and (4.6), we get that

$$d(x,x')+d(y,y') \leq \frac{d(x,x')+d(y,y')}{2s} < d(x,x')+d(y,y')$$

it is a contradiction. Therefore $(x,y) = (x',y')$ is the unique coupled fixed point of f in X. □

Proposition 4.2. Let (X,d) be a b-metric space with coefficient $s \geq 1$ and $f,g : X \times X \to X$ be two maps. Assume that the pair (f,g) is generalized rational type $\mathcal{Z}$-contraction maps. Then (u,v) is a coupled fixed point of f if and only if (u,v) is a coupled fixed point of g. Moreover, (u,v) is unique in this case.

Proof . Let (u,v) be a coupled fixed point of f. Then $u = f(u,v)$ and $v = f(v,u)$. Suppose that $u \neq g(u,v)$. We now consider

$$\zeta(s^3 d(u,g(u,v)), M(u,v,u,v)) = \zeta(s^3 d(f(u,v),g(u,v)), M(u,v,u,v)) \geq 0, \tag{4.7}$$

where
$M(u,v,u,v) = \max\{\frac{d(u,u)+d(v,v)}{2s}, \frac{d(u,f(u,v))d(u,g(u,v))}{1+d(u,u)+d(v,v)+d(u,f(u,u))}, \frac{d(u,f(u,v))d(u,g(u,v))}{1+d(u,u)+d(v,v)+d(u,f(u,u))},$
$\frac{d(f(u,v),g(u,v))d(u,u)}{1+d(u,u)+d(v,v)+d(u,f(u,u))}, \frac{d(f(u,v),g(u,v))d(v,v)}{1+d(u,u)+d(v,v)+d(u,f(u,u))}, \frac{d(u,g(u,v))d(v,v)}{1+d(u,u)+d(v,v)+d(u,f(u,u))},$
$\frac{d(u,f(u,v))d(u,u)}{1+d(u,u)+d(v,v)+d(u,f(u,u))}, \frac{d(u,f(u,v))d(v,v)}{1+d(u,u)+d(v,v)+d(u,f(u,u))},$
$\max\{d(u,f(u,v)), d(f(u,v),g(u,v))\}\} = d(u,g(u,v)).$

From the inequality (4.7), we have

$$0 \leq \zeta(s^3 d(u,g(u,v)), M(u,v,u,v)) = d(u,g(u,v)) - s^3 d(u,g(u,v)),$$

which is a contradiction. Therefore $u = g(u,v)$. Similarly, we can prove that $v = g(v,u)$. Hence, (u,v) is a coupled fixed point of g.

In the similar lines as above, it is easy to see that (u,v) is a coupled fixed point of f whenever (u,v) is a coupled fixed point of g. Let $(u,v),(u',v') \in X \times X$ be two coupled fixed points of f and g with $(u.v) \neq (u',v')$. We consider

$$\zeta(s^3 d(u,u'), M(u,v,u',v')) = \zeta(s^3 d(f(u,v),g(u',v')), M(u,v,u',v')) \geq 0,$$

where
$M(u,v,u',v') = \max\{\frac{d(u,u')+d(v,v')}{2s}, \frac{d(u,f(u,v))d(u',g(u',v'))}{1+d(u,u')+d(v,v')+d(u',f(u,v))}, \frac{d(u',f(u,v))d(x,g(u',v'))}{1+d(u,u')+d(v,v')+d(u',f(u,v))},$
$\frac{d(f(u,v),g(u',v'))d(u,u')}{1+d(u,u')+d(v,v')+d(u',f(u,v))}, \frac{d(f(u,v),g(u',v'))d(v,v')}{1+d(u,u')+d(v,v')+d(u',f(u,v))},$
$\frac{d(u',g(u',v'))d(v,v')}{1+d(u,u')+d(v,v')+d(u',f(u,v))}, \frac{d(u',f(u,v))d(u,u')}{1+d(u,u')+d(v,v')+d(u',f(u,v))},$
$\frac{d(u',f(u,v))d(v,v')}{1+d(u,u')+d(v,v')+d(u',f(u,v))}, \max\{d(u',f(u,v)), d(f(u,v),g(u',v'))\}\}$
$\leq \max\{\frac{d(u,u')+d(v,v')}{2s}, d(u,u')\}.$

If $M(u,v,u',v') = d(u,u')$ then we have

$$\zeta(s^3 d(u,u'), M(u,v,u',v')) = d(u,u') - s^3 d(u,u') \geq 0,$$

which is a contradiction. Therefore

$$d(u,u') \leq \frac{d(u,u')+d(v,v')}{2s}. \tag{4.8}$$

Similarly, we can prove that

$$d(v,v') \leq \frac{d(u,u')+d(v,v')}{2s}.. \tag{4.9}$$

Adding the inequalities (4.8) and (4.9), we get that

$$d(u,u') + d(v,v') \leq \frac{d(u,u')+d(v,v')}{2s} < d(u,u') + d(v,v'),$$

it is a contradiction.
Therefore $(u,v) = (u',v')$ is the unique coupled fixed point of f and g in X. □

Theorem 4.3. Let (X,d) be a complete b-metric space with coefficient $s \geq 1$ and the pair (f,g) be a generalized rational type $\mathcal{Z}$-contraction maps. Then f and g have a unique coupled fixed point in X.

Proof . Let x_0 and y_0 be arbitrary points in X. We define $x_{2i+1} = f(x_{2i}, y_{2i}), y_{2i+1} = f(y_{2i}, x_{2i})$ and $x_{2i+2} = g(x_{2i+1}, y_{2i+1}), y_{2i+2} = g(y_{2i+1}, x_{2i+1})$ for $i = 0,1,2,\ldots$. We consider

$$\zeta(s^3 d(x_{2n+1}, x_{2n+2}), M(x_{2n}, y_{2n}, x_{2n+1}, y_{2n+1})) = \zeta(s^3 d(f(x_{2n}, y_{2n}), g(x_{2n+1}, y_{2n+1})), M(x_{2n}, y_{2n}, x_{2n+1}, y_{2n+1})) \geq 0, \tag{4.10}$$

where
$M(x_{2n}, y_{2n}, x_{2n+1}, y_{2n+1}) = \max\{\frac{d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})}{2s},$
$\frac{d(x_{2n},f(x_{2n},y_{2n}))d(x_{2n+1},g(x_{2n+1},y_{2n+1}))}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},$
$\frac{d(x_{2n+1},f(x_{2n},y_{2n}))d(x_{2n},g(x_{2n+1},y_{2n+1}))}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},$
$\frac{d(f(x_{2n},y_{2n}),g(x_{2n+1},y_{2n+1}))d(x_{2n},x_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},$
$\frac{d(f(x_{2n},y_{2n}),g(x_{2n+1},y_{2n+1}))d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},$

$$\begin{aligned}
&\frac{d(x_{2n+1},g(x_{2n+1},y_{2n+1}))d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},\\
&\frac{d(x_{2n+1},f(x_{2n},y_{2n}))d(x_{2n},x_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},\\
&\frac{d(x_{2n+1},f(x_{2n},y_{2n}))d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},f(x_{2n},y_{2n}))},\\
&\max\{d(x_{2n+1},f(x_{2n},y_{2n})),d(f(x_{2n},y_{2n}),g(x_{2n+1},y_{2n+1}))\}\}\\
=\max\{&\frac{d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})}{2s},\\
&\frac{d(x_{2n},x_{2n+1})d(x_{2n+1},x_{2n+2})+d(x_{2n+1},x_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+1})d(x_{2n},x_{2n+2})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+2})d(x_{2n},x_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+2})d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+2})d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+1})d(x_{2n},x_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\frac{d(x_{2n+1},x_{2n+1})d(y_{2n},y_{2n+1})}{1+d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})+d(x_{2n+1},x_{2n+1})},\\
&\max\{d(x_{2n+1},x_{2n+1}),d(x_{2n+1},x_{2n+2})\}\}\\
\le\max\{&\frac{d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})}{2s},d(x_{2n+1},x_{2n+2})\}.
\end{aligned}$$

If $M(x_{2n},y_{2n},x_{2n+1},y_{2n+1})=d(x_{2n+1},x_{2n+2})$ then from (4.10), we have

$$\begin{aligned}
0\le\zeta(s^3d(x_{2n+1},x_{2n+2}),M(x_{2n},y_{2n},x_{2n+1},y_{2n+1}))&=\zeta(s^3d(x_{2n+1},x_{2n+2}),d(x_{2n+1},x_{2n+2}))\\
&<d(x_{2n+1},x_{2n+2})-s^3d(x_{2n+1},x_{2n+2}),
\end{aligned}$$

which is a contradiction. Therefore

$$d(x_{2n+1},x_{2n+2})\le\frac{d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})}{2s}\tag{4.11}$$

for all $n=0,1,2,\ldots$.

Similarly, we can prove that

$$d(y_{2n+1},y_{2n+2})\le\frac{d(y_{2n},y_{2n+1})+d(x_{2n},x_{2n+1})}{2s}\tag{4.12}$$

for all $n=0,1,2,\ldots$. Adding the inequalities (4.11) and (4.12), we have

$$d(x_{2n+1},x_{2n+2})+d(y_{2n+1},y_{2n+2})\le h[d(x_{2n},x_{2n+1})+d(y_{2n},y_{2n+1})],$$

where $h=\frac{1}{2s}<1$. Also, it is easy to see that

$$d(x_{2n+2},x_{2n+3})+d(y_{2n+2},y_{2n+3})\le h[d(x_{2n+1},x_{2n+2})+d(y_{2n+1},y_{2n+2})].$$

Therefore

$$d(x_n,x_{n+1})+d(y_n,y_{n+1})\le h[d(x_{n-1},x_n)+d(y_{n-1},y_n)],$$

for all $n=1,2,3,\ldots$. Continuing in the same way, we get that

$$d(x_n,x_{n+1})+d(y_n,y_{n+1})\le h^n[d(x_0,x_1)+d(y_0,y_1)].$$

For $m>n,m,n\in\mathbb{N}$, we have

$$\begin{aligned}
d(x_n,x_m)+d(y_n,y_m)&\le s[d(x_n,x_{n+1})+d(x_{n+1},x_m)]+s[d(y_n,y_{n+1})+d(y_{n+1},y_m)]\\
&\le s[d(x_n,x_{n+1})+d(y_n,y_{n+1})]+s^2[d(x_{n+1},x_{n+2})+d(x_{n+2},x_m)]\\
&\quad+s^2[d(y_{n+1},y_{n+2})+d(y_{n+2},y_m)]\\
&=s[d(x_n,x_{n+1})+d(y_n,y_{n+1})]+s^2[d(x_{n+1},x_{n+2})+d(y_{n+1},y_{n+2})]\\
&\quad+s^2[d(x_{n+2},x_m)+d(y_{n+2},y_m)]\ldots+s^{m-n}[d(x_{m-1},x_m)+d(y_{m-1},y_m)]\\
&\le[sh^n+s^2h^{n+1}+\ldots+s^{m-n}h^{m-1}][d(x_0,x_1)+d(y_0,y_1)]\\
&\le sh^n[1+sh+(sh)^2\ldots+(sh)^{m-1}+\ldots][d(x_0,x_1)+d(y_0,y_1)]\\
&=sh^n(\tfrac{1}{1-sh})[d(x_0,x_1)+d(y_0,y_1)]\to0\text{ as }n\to\infty.
\end{aligned}$$

Therefore $\{x_n\}$ and $\{y_n\}$ are b-Cauchy sequences in X. Since X is b-complete, there exist $x,y\in X$ such that $x_n\to x$ and $y_n\to y$ as $n\to\infty$. We now prove that $x=f(x,y)$ and $y=f(y,x)$. On the contrary suppose that $x\ne f(x,y)$ and $y\ne f(y,x)$. We now consider

$$\begin{aligned}
\zeta(s^3d(f(x,y),x_{2n+2}),M(x,y,x_{2n+1},y_{2n+1}))&=\zeta(s^3d(f(x,y),g(x_{2n+1},y_{2n+1})),\\
&\quad M(x,y,x_{2n+1},y_{2n+1}))\ge0,
\end{aligned}\tag{4.13}$$

where

$$M(x,y,x_{2n+1},y_{2n+1}) = \max\{\frac{d(x,x_{2n+1})+d(y,y_{2n+1})}{2s}, \frac{d(x,f(x,y))d(x_{2n+1},g(x_{2n+1},y_{2n+1}))}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(x_{2n+1},f(x,y))d(x,g(x_{2n+1},y_{2n+1}))}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(f(x,y),g(x_{2n+1},y_{2n+1}))d(x,x_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(f(x,y),g(x_{2n+1},y_{2n+1}))d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(x_{2n+1},g(x_{2n+1},y_{2n+1}))d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(x_{2n+1},f(x,y))d(x,x_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(x_{2n+1},f(x,y))d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\max\{d(x_{2n+1},f(x,y)), d(f(x,y),g(x_{2n+1},y_{2n+1}))\}\}$$
$$= \max\{\frac{d(x,x_{2n+1})+d(y,y_{2n+1})}{2s}, \frac{d(x,f(x,y))d(x_{2n+1},x_{2n+2})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(x_{2n+1},f(x,y))d(x,x_{2n+2})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(f(x,y),x_{2n+2})d(x,x_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(f(x,y),x_{2n+2})d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(x_{2n+1},x_{2n+2})d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\frac{d(x_{2n+1},f(x,y))d(x,x_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))}, \frac{d(x_{2n+1},f(x,y))d(y,y_{2n+1})}{1+d(x,x_{2n+1})+d(y,y_{2n+1})+d(x_{2n+1},f(x,y))},$$
$$\max\{d(x_{2n+1},f(x,y)), d(f(x,y),x_{2n+2})\}\}.$$

On taking limit superior as $n \to \infty$ in $M(x,y,x_n,y_n)$ and using Lemma 2.7, we have

$$\limsup_{n\to\infty} M(x,y,x_n,y_n) \leq sd(x,f(x,y)).$$

On letting limit superior as $n \to \infty$ in (4.13) and using the Lemma 2.7, we have

$$0 \leq \limsup_{n\to\infty} \zeta(s^3 d(f(x,y),x_{2n+2}), M(x,y,x_{2n+1},y_{2n+1}))$$
$$= \limsup_{n\to\infty} M(x,y,x_{2n+1},y_{2n+1}) - \liminf_{n\to\infty} s^3 d(f(x,y),x_{2n+2})$$
$$\leq sd(x,f(x,y)) - s^3 \tfrac{d(x,f(x,y))}{s},$$

a contradiction. Therefore $x = f(x,y)$. Similarly we can prove that $y = f(y,x)$. Therefore (x,y) is a coupled fixed point of f. By Proposition 4.2, we have (x,y) is a unique common coupled fixed point of f and g in X. □

5 Corollaries and examples

Corollary 5.1. Let (X,d) be a complete b-metric space with coefficient $s \geq 1$. $f : X \times X \to X$ be two maps. Assume that there exist two continuous functions $\varphi, \psi : [0,\infty) \to [0,\infty)$ with $\varphi(t) < t \leq \psi(t)$ for all $t > 0$ and $\varphi(t) = \psi(t) = 0$ if and only if $t = 0$ such that

$$\psi(s^d(f(x,y),f(u,v))) \leq \varphi(M(x,y,u,v))$$

where

$$M(x,y,u,v) = \max\{\frac{d(x,u)+d(y,v)}{2s}, \frac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\frac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\frac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\max\{d(u,f(x,y)), d(f(x,y),f(u,v))\}\}, \text{ for all } x,y,u,v \in X.$$

Then f has a unique common coupled fixed point in X.

Proof . Follows from Theorem 4.1 by choosing $\zeta(s,t) = \varphi(t) - \psi(t)$ for all $t,s \in [0,\infty)$. □

Corollary 5.2. Let (X,d) be a complete b-metric space with coefficient $s \geq 1$. $f,g : X \times X \to X$ be two maps. Assume that there exist two continuous functions $\varphi, \psi : [0,\infty) \to [0,\infty)$ with $\varphi(t) < t \leq \psi(t)$, for all $t > 0$ and $\varphi(t) = \psi(t) = 0$ if and only if $t = 0$ such that

$$\psi(s^d(f(x,y),g(u,v))) \leq \varphi(M(x,y,u,v))$$

where

$$M(x,y,u,v) = \max\{\frac{d(x,u)+d(y,v)}{2s}, \frac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\frac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\frac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \frac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))},$$
$$\max\{d(u,f(x,y)), d(f(x,y),g(u,v))\}\}, \text{ for all } x,y,u,v \in X.$$

Then f and g have a unique common coupled fixed point in X.

Proof . Follows by taking $g = f$ in Corollary 5.1. □

The following is an example in support of Theorem 4.1.

Example 5.3. Let $X = [0, 1]$ and let $d : X \times X \to \mathbb{R}^+$ defined by

$$d(x, y) = \begin{cases} 0 & \text{if } x = y \\ (x + y)^2 & \text{if } x \neq y. \end{cases}$$

Then clearly (X, d) is a b-metric space with coefficient $s = 2$. We define $f, g : X \times X \to X$ by

$$f(x, y) = \begin{cases} \frac{x^2+y^2}{16} & \text{if } x, y \in [0, \frac{1}{2}) \\ \frac{1}{32} & \text{if } x, y \in [\frac{1}{2}, 1] \\ 0 & \text{otherwise} \end{cases}$$

$\zeta : \mathbb{R}^+ \times \mathbb{R}^+ \to (-\infty, \infty)$ by $\zeta(t, s) = \frac{99}{100}s - t, t \geq 0, s \geq 0$.

Case (i). $x, y, u, v \in [0, \frac{1}{2})$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{x^2+y^2}{16} + \tfrac{u^2+v^2}{16}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), f(u, v))\}\}). \end{aligned}$$

Case (ii). $x, y, u, v \in [\frac{1}{2}, 1]$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{1}{32} + \tfrac{1}{32}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), f(u, v))\}\}). \end{aligned}$$

Case (iii). $x, y \in [\frac{1}{2}, 1], u, v \in [0, \frac{1}{2})$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{1}{32} + \tfrac{u^2+v^2}{16}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), f(u, v))\}\}). \end{aligned}$$

Case (iv). $x, y \in [0, \frac{1}{2}), u, v \in [\frac{1}{2}, 1]$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{x^2+y^2}{16} + \tfrac{1}{32}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,f(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),f(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), f(u, v))\}\}). \end{aligned}$$

Therefore f satisfy all the hypothesis of Theorem 4.1 and $(0, 0)$ is a unique coupled fixed point of f.

The following is an example in support of Theorem 4.3.

Example 5.4. Let $X = [0, 1]$ and let $d : X \times X \to \mathbb{R}^+$ defined by

$$d(x, y) = \begin{cases} 0 & \text{if } x = y \\ (x + y)^2 & \text{if } x \neq y. \end{cases}$$

Then clearly (X, d) is a b-metric space with coefficient $s = 2$. We define $f, g : X \times X \to X$ by

$$f(x, y) = \begin{cases} \frac{\log(1+x+y)}{16} & \text{if } x, y \in [0, \frac{1}{2}) \\ \frac{1}{32} & \text{if } x, y \in [\frac{1}{2}, 1] \end{cases}$$

and

$$g(x, y) = \begin{cases} \frac{xye^{xy}}{8} & \text{if } x, y \in [0, \frac{1}{2}) \\ \log(x + y) & \text{if } x, y \in [\frac{1}{2}, 1]. \end{cases}$$

$\zeta : \mathbb{R}^+ \times \mathbb{R}^+ \to (-\infty, \infty)$ by $\zeta(t, s) = \frac{99}{100}s - t, t \geq 0, s \geq 0$.

Case (i). $x, y, u, v \in [0, \frac{1}{2})$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{\log(1+x+y)}{16} + \tfrac{uve^{uv}}{8}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), g(u, v))\}\}). \end{aligned}$$

Case (ii). $x, y, u, v \in [\frac{1}{2}, 1]$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{1}{32} + \log(u + v)]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), g(u, v))\}\}) \end{aligned}$$

Case (iii). $x, y \in [\frac{1}{2}, 1], u, v \in [0, \frac{1}{2})$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{1}{16} + \tfrac{uve^{uv}}{8}]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), g(u, v))\}\}) \end{aligned}$$

Case (iv). $x, y \in [0, \frac{1}{2}), u, v \in [\frac{1}{2}, 1]$.

$$\begin{aligned} s^3 d(f(x, y), g(u, v)) &= 8[\tfrac{\log(1+x+y)}{8} + \log(x + y)]^2 \\ &\leq \tfrac{99}{400}[(x + u)^2 + (y + v)^2] \\ &= \tfrac{99}{100}(\tfrac{d(x,u)+d(y,v)}{2s}) \\ &\leq \tfrac{99}{100}(\max\{\tfrac{d(x,u)+d(y,v)}{2s}, \tfrac{d(x,f(x,y))d(u,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(x,g(u,v))}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(f(x,y),g(u,v))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(f(x,y),g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,g(u,v))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \tfrac{d(u,f(x,y))d(x,u)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \tfrac{d(u,f(x,y))d(y,v)}{1+d(x,u)+d(y,v)+d(u,f(x,y))}, \\ &\quad \max\{d(u, f(x, y)), d(f(x, y), g(u, v))\}\}) \end{aligned}$$

Therefore the pair (f, g) satisfy all the hypotheses of Theorem 4.3 and $(0, 0)$ is a unique common coupled fixed point of f and g.

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Analyzing the Effect of Uncertainty in Low Power SRAM Cells using Artificial Intelligence Technique

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This paper addresses the uncertainty that is present in the design of static random access memory (SRAM) cells using an artificial intelligence (AI) technique. The SRAM has much uncertainty in high-performance portable very large-scale integration (VLSI) chips due to their performance and storage density. This paper presents the way for solving the uncertainty problem by evaluating point-by-point recreation derived for the memory cells inform of the power, speed, and area investment funds acquired in the advanced cell configuration when contrasted with the standard regular architecture for autonomous vehicles using AI algorithm. The adiabatic low power technique is implemented to enrich the configuration of the 6T-SRAM cells. The procedure of the adiabatic process will provide high loss in terms of dissipation of energy which is connected to ground (0V) and transition can be converted from '1' to '0'. Moreover, this transition will be decreased to a high amount of degree within corresponding memory cells. Thus uncertainties with the AI model can able to deliver low power reduction using the automatic model of operation as standard adiabatic 6T SRAM cells are implemented. To prove the effectiveness in

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the reduction of uncertainties a low power margin is obtained with marginal values of 0.25 Volts which is much lesser than the existing models.

Keywords: SRAM; 6T-SRAM cell; adiabatic power; energy dissipation; power reduction; delay.

1. Low Power Uncertainties — An Introduction

Most of the uncertainties that are present in memories are used for storing data or information. Generally, two types of memories are preferred in electronic memory devices such as volatile and non-volatile memories based on applications, these memories affect the performance of speed of the devices. In recent years, the static random access memory (SRAM) is one of the substantial pieces of research for the development of the speed of the process, reducing the memory and power due to increasing demand on advanced electronic devices such as laptops, integrated circuit (IC) memory cards, etc.[1,2] The feedback cells are designed to improve the performance of the memory cells.[3–9] These are widely used in on/off-chip memories mobile applications of low standby leakage. The static memory is the semiconductor memory work with bistable latching circuitry, which stores each bit and exhibits the data remembrance. The static memories are volatile memory, that store data eventually lost when not powered in the memory cell.

1.1. *Uncertainty in SRAM cell design: Survey model*

The SRAMs are used for solving several uncertainties that are present in various microelectronics applications like advanced server processors, system on chip (SoC) and multimedia applications. These are operating at low power supplies with high noise immunity due to large noise margins. The embedded SRAM in SoC products are designed for handling the processors easily and effectively.[10] The various chips are designed based on the demand for performance, saving memory within less size and minimizing the latency with the integrated fast memories (cache) are being integrated on-die. Many researchers are suggested SRAM designed for SoC applications and high-performance processors. The memory element or storage element is one of the basic operations of the SRAM cell, it includes the writing and reading operation from/into the cell. In this paper, implement the technique for advanced SRAM design aspects, basic operations of existing 6T-SRAM (six transistors) memory cell and design process, nano-regime techniques and challenges, limitations in read-write requirements of memory cells. This performance is evaluated by the two design metrics such as read static noise margin (RSNM) and write static noise margin (WSNM). Apart from these parameters, the inline metric, N-curves also used to measure the stability of reading and write operation of the memory.[11,12]

The basic SRAM cells work with feedback mechanism-based cross-coupled inverters to maintain their state. The dynamic random access memory (DRAM) cells hold a charge as data, which acts as a floating capacitor. The data is regularly retrieved by dynamic cells and charge stored leaky floating capacitor. The

charges stored in the leaky floating capacitor and dynamic cells are refreshed regularly to retrieve the stored data. The high-performance read and write operations are achieved by the cross-coupled inverters in SRAM. However, these static memories are faster compared with dynamic RAM, it requires much space (area) than DRAMs. The SRAM cache memory contains sense amplifiers, an address decoder, an array of memory, and write drivers to enable the writing into and reading from the array of memory. The standard memory architecture is shown in Fig. 1. These SRAM memory arrays exit with $2n$ words of 2m bits each. Every bit is stored in the memory cell and share bit-line pairs (BL, BL′) in each column and a common word-line (WL) in each row. The access of the cell is performed by the resistances and capacitances of the bit lines and word lines. The size of the memory is proportional to the number of rows and columns.[8,9] The folded technology is used high-level memories, including the bit line capacitance, the word line capacitance consists of $2n - k$ rows and $2m + k$ columns and in each row of the memory with $2k$ words. The SRAM cells are addressed by the selection of appropriate lines like word line, a bit line pairs are activated with the row and a column decoder.

1.1.1. *Recent literature*

The process of accruing uncertainties is explained using a factorial model[13] where the minimum and maximum values are defined. This provides a clear insight in achieving suitable values which are defined in terms of variance. But in field intensity, both limits do not establish any security for adiabatic cell structures. Subsequent procedures are carried out for quantification uncertainties[14] which are used for predicting space with high limit boundaries. In this case, more amount of limitations leads to prediction problems which indicate the failure of the automatic process. Therefore, for high limit boundaries a probability model is defined which holds all quantified processes for 5T and 6T SRAM structures.[15]

1.2. *Deciphering uncertainties using AI*

Artificial intelligence (AI) techniques are implemented for solving the uncertainties that are present in low-power SRAM design. Since in the proposed method low-power SRAM cells are designed they can be applied in all applications of the Internet of Things (IoT) since the metal oxide semiconductor field effect transistor (MOSFET) has many limitations. To be precise the SRAM design memory requirements are tested with an autonomous vehicle that turns with battery-packed systems. To analyze the aforementioned effect a non-linear classification problem is applied with perceptron algorithms where the basic form is represented using mathematical equations as follows:

$$P_i = \begin{cases} 0 & \text{if input } < d_i, \\ 1 & \text{if input } > d_i, \end{cases} \tag{1}$$

where d_i represents the decision line which is calculated from input of AND gate.

If the values of decision variables are calculated then the function of perceptron can be defined using three different variables as represented in Eq. (2).

$$f(P_i) = \sum_{i=1}^{n} \vartheta_i * y_i + \tau_i, \tag{2}$$

where ϑ_i, y_i and τ_i represents the input load, path followed and preconception of perceptron.

Equation (2) represents that bias points is primarily implemented for shifting the lines between two different cases, namely, 0 and 1. In the modeling of deep neural networks with SRAM cells the major objective in autonomous vehicles is to reduce the amount of loss that is present in the system. Therefore, the objective function can be defined using Eq. (3) as

$$O(i) = \int_{i=1}^{n} P(i,n) * \mu(i,n) didn \tag{3}$$

where $\mu(i,n)$ represents the loss function.

In case if loss function is much higher then it should be optimized by converting it to a gradient function which is represented using Eq. (4).

$$O_{\text{modified}}(i) = \frac{1}{\sigma} \sum_{i=1}^{n} \mu(i,n), \tag{4}$$

where σ represents the gradient function.

Equation (4) represents the modified objective function with reduction in loss terms. Since the method implements a binary variable the same function can be represented using sigmoid function as follows:

$$f_{\text{modified}}(P_i) = e^{-in} \frac{1}{1+e^{-in}}, \tag{5}$$

where e^{-in} represents the exponential function of two variable functions.

Using AI model the problem of uncertainties for data distribution with low power 5T and 6T cells can be solved by minimum and maximum set of arrays using the following equation. This set of arrays is suitable for random data set with distinct variance value as uniform distribution can be achieved in this case.

$$D_i(\text{variance}) = \sum_{i=1}^{n} |v_i - v_n|^2 \tag{6}$$

where v_i and v_n denotes the variance with quantization of data which is used for reducing the power that is transmitted for 5T and 6T cell data.

1.3. *Solving uncertainties: Proposed methodology*

From conventional technique analysis, it has been established that many procedures of low power design using SRAM cells have not been developed based on the automation model. However, several processes provide an advantage in manual

mode of operation which includes an SoC technology for avoiding high power that is supplied in a single cell. But manual adjustment of power will not guarantee an adiabatic reduction in the proposed cell RAM design, thus, as a result it leads to uncertainty in SRAM systems. To prevent uncertainties an automatic mode of operation is assured using AI systems where perceptron algorithms are integrated for solving all non-classified problems. In addition, three different operating modes are introduced as uncertainties will be different in the case of 5T and 6T cell structures.

1.4. *Objectives*

The major objective of the proposed work is divided into a multi-objective case study that solves the following problems that exist in conventional models.

- To solve the uncertainties that are present in adiabatic cells by replacing SoC technology with AI models.
- To integrate the proposed model using frame structure with reduced power infrastructure for SRAM cells.
- To provide a low noise margin which is less than 1V for 5T and 6T cells by shifting binary values 0 and 1.

2. Design Model of Uncertainties

In very large-scale integration (VLSI) designs, the static random access constitutes a large area, which contains thousands of transistors are in a single cell. In these present days, the SRAM cell designs with minimum size transistors for high packing density.[5] For the past three decades, scaling processing is done for the reduction of the size of cell.[6] SRAM takes designs with two primary aspects power dissipation and delays in reading and writing operations in SRAM. The dynamic power dissipated with the read/write operation.[7] Figure 1 is the standard 6T (six transistors) CMOS static memory cell is illustrated schematically.

The transistors in cells M1, M2, M3 and M4 are cross-coupled inverters, which act as storage elements. The intention SRAM design effort is directed to decrease the

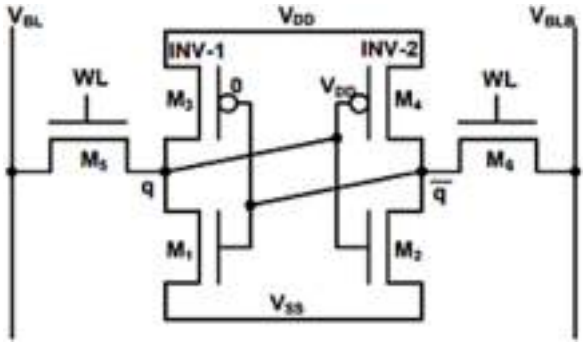

Fig. 1. Standard 6T SRAM cell.

power consumption and area of the cell. The millions of cells can be built in a small chip. The sub-threshold leakage currents are controlled by the power consumption level of the cell and memory circuits are handled by the large threshold voltage. The various scaling techniques are implemented for MOSFET to better enhance the performance of the SRAM cell. The MOSFET controlled with gate oxide leakage, ultra-shallow, control of abrupt junction and short channel effects implement SRAM scaling for SI MOSFET structure. The bulk sub-45 nm chip control of SCE with heavy super-halo implants and doping is implemented to prevent the leakage currents from sub-surface.[15] The impurity scattering carrier motilities are degraded and high transverse electric field in the ON-state. The degradation of short channel results in large leakage and sub-threshold slope. The variable threshold voltage is the new technique for random dopant fluctuation to nano scalable bulk-Si MOSFETs. Including this, the line-edge roughness and statistical dopant fluctuations increase the spread in variable threshold levels in the transistor and on-off currents and can limit the size of the cache.[13]

Figure 2 shows the voltage transfer characteristics (VTCs) of cross-coupled inverters. The read and write operation of the SRAM cell can be performed by the cross-coupled inverters of VTC. In this process, the stored values are controlled to the two stable states. In SRAM cell flip internal state, the current state internal crosses the switching threshold value (Vs). This state is not disturbing in the read operation, it forces swing from internal voltage to change the state into write operation.

2.1. *5T SRAM cell*

Figure 3 shows the proposed 5T-SRAM CELL design, the features are related to basic 6T cell except for the lack of an access transistor to perform the tasks are indistinguishable to 6T SRAM cell.[16,17] The proposed SRAM memory cell requires five transistors for solving the uncertainties, so eventually, reduces the area in the

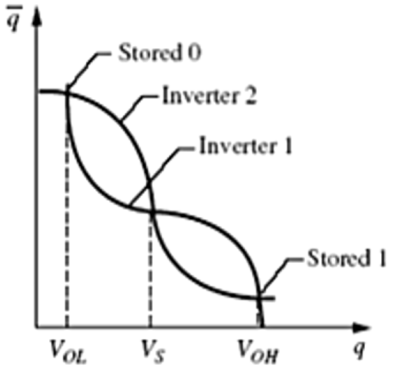

Fig. 2. VTC of SRAM.

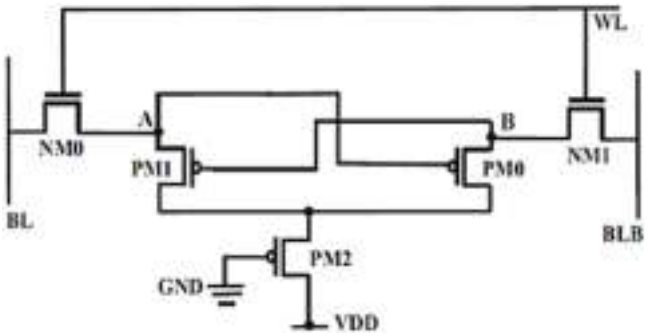

Fig. 3. 5T-SRAM cell diagram.

5T SRAM cell. The power dissipation and delay are also less compared with other existing SRAM cells with acceptable stability, which is based on noise margin.[18]

3. Source of Uncertainties and Operating Modes

(1) Write mode: The SRAM performs the write operation when WL = 1. Then NM0 and NM1 are turned in to "ON" states. The transistors output nodes "A" and "B" are connected to PM0 and PM1 transistors gate respectively. When WL = 0, the BLB and BL should be set as logic '1' and logic '0'. When "A" states '0, then PM2 is "ON". When it switches to the "ON" state, the output node "B" and PM0 connect to the power supply V_{dd} through PM2.

(2) Read mode: In this mode, the proposed operation is different than 6T-SRAM. Instead of logic '1', logic '0 is applied to bit line and set as WL = 1. If WL = 1 then, NM0 and NM1 transistors are turned into an 'ON' states. The Node "A" = 1, which holds the logic '1', it charges the bit line to '1' for weak 1 due to NM1.

If the node "B" is "0FF", which holds '0" but will be pulled to logic '0'. The voltage level at BL is greater than BLB, which is detected by the sense amplifier and it gives logic '1'. Similarly, at nodes A = 0, B = 1, the BLB voltage is higher than BL voltage, sense amplifier output changed to logic '0'.

(3) Hold mode: The proposed cell operated with hold mode when WL0. In the write mode of the cell, node stores weak '1' at the node "A" = 1 due to the NM0 access transistor, which is a weak passer of 1. The two transistors (NM0 and NM1) are "OFF" conditions when WL = 0. The corresponding node "A" holds the weak '1' and node "B" handles the strong '0', respectively.

Node B changed into strong '1', when node "B" turned on to switch on and power supply voltage PM2 is also ON, which is known as a strong passer of 1. Figure 4 shows the simulated response for the proposed memory cell in reading and write mode (WL = 1) and hold (WL = 0) state with the same size as the transistors.

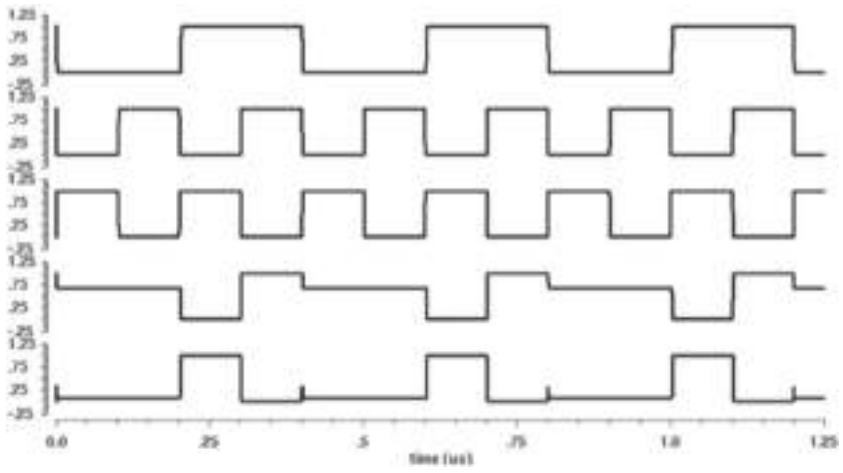

Fig. 4. Simulated response of proposed cell.

3.1. *Adiabatic 6T-SRAM cell*

The adiabatic switching process is performed by the switching operations to maintain the small potential between the switching devices.[19,21] In conventional switching cases, the potential Vr is high between the switch resistances to the abrupt application of V_{dd} to the RC circuit. This variation can be performed by the capacitor charging from a time-varying source.

Initially, $Vi = 0\,\mathrm{V}$. The ramp slightly increases up to V_{dd} *with* a slew rate $Vr = Vi - Vc$, which is set by ensuring that its period $T \gg \mathrm{RC}$. The corresponding energy dissipated as follows:

$$E_{\mathrm{diss}} = I^2\mathrm{RT} = (CV_{\mathrm{dd}}/T)^{2\mathrm{RT}} = (\mathrm{RC}/T)C(V_{\mathrm{dd}})^2.$$

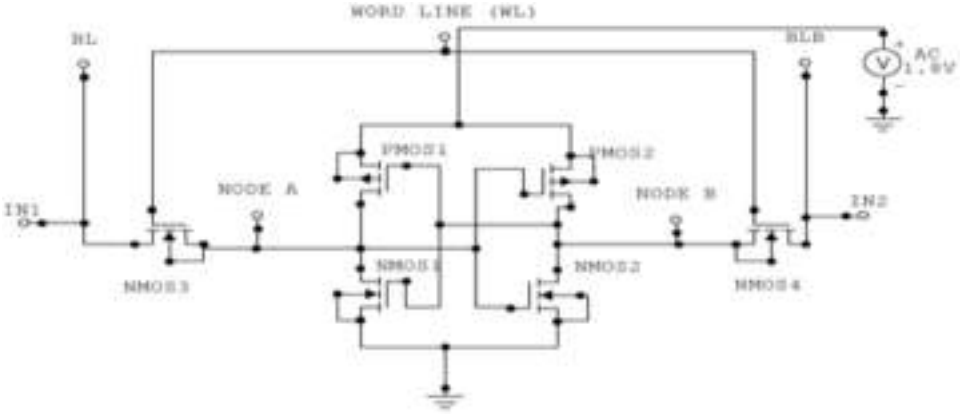

Fig. 5. Proposed adiabatic 6T-SRAM design.

The power dissipation decreases with an increasing linear increase in T. The adiabatic discharge formed a similar manner with decreasing ramp. If 'T' $\gg$ RC, then the energy dissipation during charging Ediss _ 0 and the total energy removed from the supply is $^1/_2$ $C(V_{\mathrm{dd}})^2$ — the minimum charge required the capacitor and hence hold the logic state. In the cell adiabatic process, the energy is eliminated from the capacitor and back to the supply in the discharge cycle, so the node capacitances charge and discharge and the average power dissipation are also reduced. Figure 5 shows the adiabatic 6T-SRAM memory cell, the dynamic switching operations can be performed by the potential across the switching devices is kept arbitrarily small. Generally, in a conventional circuit, the Vr is high due to the abrupt application of V_{dd} in RC. This process can be obtained by the power source and adiabatic charging from a time-varying source from the initial stage to the final stage.

4. Results and Discussions

This paper designed the flip flop and stored the input information with better output reconstruction. Figure 6 shows the existing method (5T-SRAM) waveform, which contains the high power and high noise margin level.

Figure 7 shows the proposed method waveform after solving uncertainties. Compare with the existing method, the noise margin level is less. The data storage is speed and required power is very less. The proposed method has less noise margin for reconstructing the original data with less power. The speed is also fast compared with the previous method.

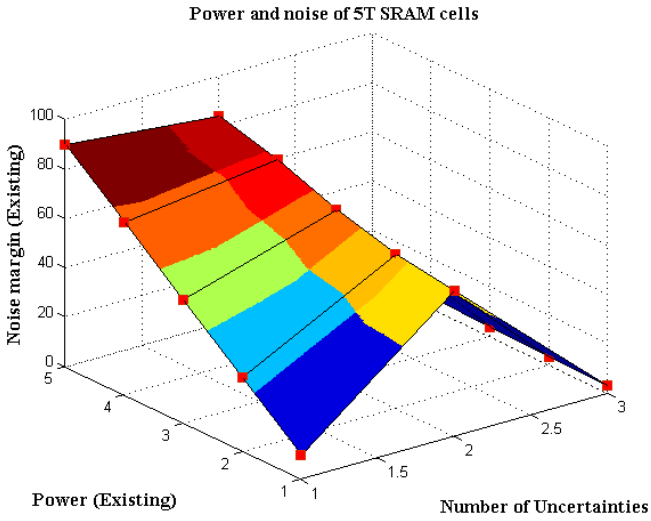

Fig. 6. Existing method performance.

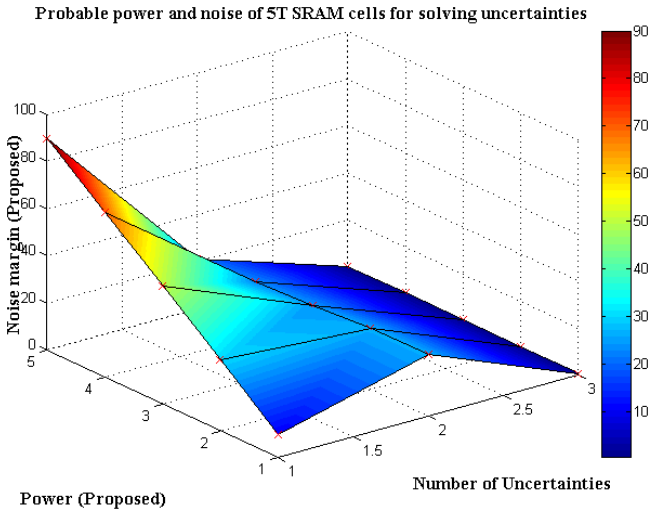

Fig. 7. Proposed method results.

5. Conclusions and Future Scope

The paper suggests a new flanged technique for solving uncertainties that are present in SRAM flip-flop design and stored the input process into the memory cell. The process of uncertainty is compared with existing methods and it is observed that the data storage process is complex due to the high noise margin. So, the uncertainty problem requires a high-power level and low-speed techniques. To overcome this limitation on uncertainties the proposed technique delivers a novel platform where the speed is more and delay is less due to the less noise margin the uncertainties are solved and this method is suitable for reading and write operations compare with other standard SRAM cells.

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